MIPS BU (Wave Computing).

Tools for optimal placement and routing in Hardware Design

Team:
Maxim Kostin
Mihail Sheinberg
Sofiia Yermolaieva

Customer:
Yuri Panchul

Document is proved and accepted by the customer _____

(signature) /(full name)

Initial Project Description

Context

The optimal placement and routing (connecting placed cells by wires) of the hardware components is the cornerstone of the physical part of design flow that determines the efficiency of the developed components. The tools by Synopsys and Cadence have the monopoly position in the development teams in Intel, Apple, NVidia and other electronic companies. The tool licenses costs can easily rich 100x K$ per node. A typical electronic design company pays millions in dollars or more in licensing fees. New tools in this domain can disrupt the monopoly and create a great market potential for a start-up.

The most immediate use of open-source electronic design automation (EDA) flow is educational and research projects in universities. Right now Electrical Engineering (EE) departments have to obtain educational licenses from Synopsys and Cadence or, alternatively, make arrangements with such organizations as Europractice that licenses EDA tools from vendors themselves. The current situation restricts the academic research and has to be changed.

Goal

The team will study a subject on the placement and routing problems and will apply optimization algorithms. The ideal solution will be a prototype that:

1. Parses Verilog netlist files (examples will be provided) into a graph of standard cells and connections.
2. Applies optimal placement and connections algorithm. The optimal placement should use the smallest number of layers of connectivity, as well as minimal overall length of the connections, with some restrictions on the longest path.
3. Displays the intermediate graph and the final result.

Constraints on the solution

1. The project shall be implemented within 4 hours (with presentation).
2. The project shall be implemented by 3 students.

Stakeholders

As a stakeholder is a person who has an impact on the project and gets a profit out of the project, our team identified the next stakeholders:

1) Customer and domain expert - Yuri Panchul
2) Team who participate in Hackathon - Maxim Kostin, Mihail Sheinberg, Sofiia Yermolaieva
3) Organizer of the Hackathon - Andrey Sadovykh

Simplification of the goal with respect to the constraints

In our hackathon we are going to use a simplified model of the standard cells. We assume that all standard cells have not only the same height, but also the same width. We also ignore in our initial implementation all physical properties of ASIC cells, including timing delays and electric power consumption.

For placement and connection we are going to use Li Algorithm. Li algorithm is rarely used in modern ASIC design. It was used in early PCB design. However we are going to use Li algorithm because its simplicity makes it practical in the time constraints of the hackathon.

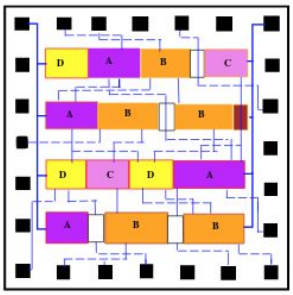
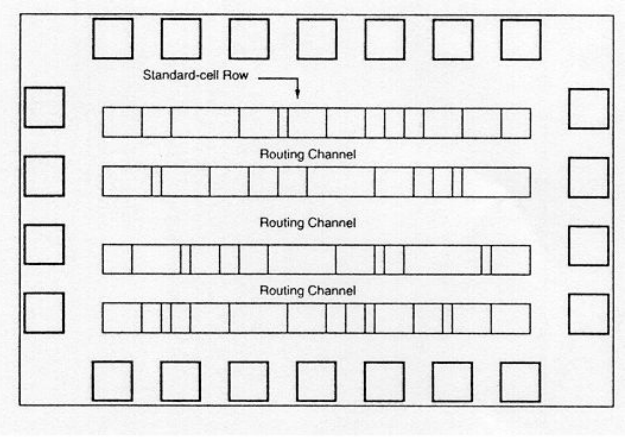
Source of the requirements

All requirements presented below are extracted from the elicitation interview with the stakeholder Yuri Panchul.

Glossary

NOTE:
The place and route algorithms can be applied to both printed-circuit boards (PCBs) or Application-Specific Integrated Circuits (ASICs). In our project we concentrate on ASICs.

Term	Definition
The Solution	It is a prototype of the system which will be developed during the hackathon.
Application-Specific Integrated Circuit (ASIC)	A specific integrated circuit. Could be represented as a chip in a printed circuit board. In our project it is used as a base for placement of programs in the representation of standard cells and connections (wires).
Logical element	A hardware block that implements a logical operation (such as AND, OR, NOT etc.) on one or more binary inputs and produces a single binary output [3].
Input signal	Is a digital signal that carries a binary value and comes into design or a cell.
Output signal	Is a digital signal that carries a binary value and comes out of a cell of a design.
Wire	In the context of out project wire is a connection between standard or I/O cells inside a chip. This connection conducts electricity and is typically made of copper or aluminum implanted inside silicon.
Standard cell	is a building block of the most popular ASIC design and manufacturing technology flow as of today. “Standard” refers to the feature of this methodology that all startd cells in a particular ASIC library have the same dimension (“height”) of the side perpendicular to the direction of power lines. This feature makes it convenient to distribute power and simplifies

	place and routing algorithms. The standard cell library (also called ASIC library) is usually supplied by a semiconductor foundry (a manufacturing fab).
Placement	Is a placement of standard cells on the ASIC.
Lee algorithm	Is one possible solution for maze routing problems based on Breadth-first search. It always gives an optimal solution, if one exists, but is slow and requires considerable memory.
Layer	It is a layer of the ASIC, the layer of copper laminated onto and/or between sheet layers of a non-conductive substrate. This term refers to the inner layers in multi-layer ASICs.
Routing channel	It is a route or track on the ASIC are used for standard cells could be placed.   [4]

Requirements to the prototype

File reader

1. The solution will provide a custom file reader.
2. The file shall start with input signals, one input signal per line.
3. After lines with input signals, output signals shall be listed.
4. After lines with output signals,logical operations shall be listed.
5. Logical operation shall contain logical gate, one or two input's ids and one output id.
   If the id of not defined output is used, then it is considered as a wire.
   Example: "*and 1 2 3"*
6. Input signal shall be denoted in the format "in " + id.
   Example: "in 1".
7. Output signal shall be denoted in the format "out " + id.
   Example: "out 1".
8. Logical gate shall be denoted in the format "%gate_name%".
   Example: "and", "or".

   Example of the file's content:
   "in 1
   in 2
   in 4
   out 6
   and 1 2 3
   or 3 4 5
   not 5 6"

Placement

1. The solution will provide placement for the standard and I/O cells.
2. The constraint for the input I/O cells: they should be placed in the top row.
3. The constraint for the output I/O cells: they should be placed in the bottom row.
4. The standard cells (which implement logical elements) can be placed in any row.
5. In the initial implementation we place standard cells randomly. Later on we are going to optimize the placement for better routing.

Routing

1. The routing of wires is going to be implemented using Lee algorithm.
2. Each wire shall not intersect other wires.
3. If no route could be constructed for a wire without intersection on each existing layer, a new layer shall be added.

Graphical representation

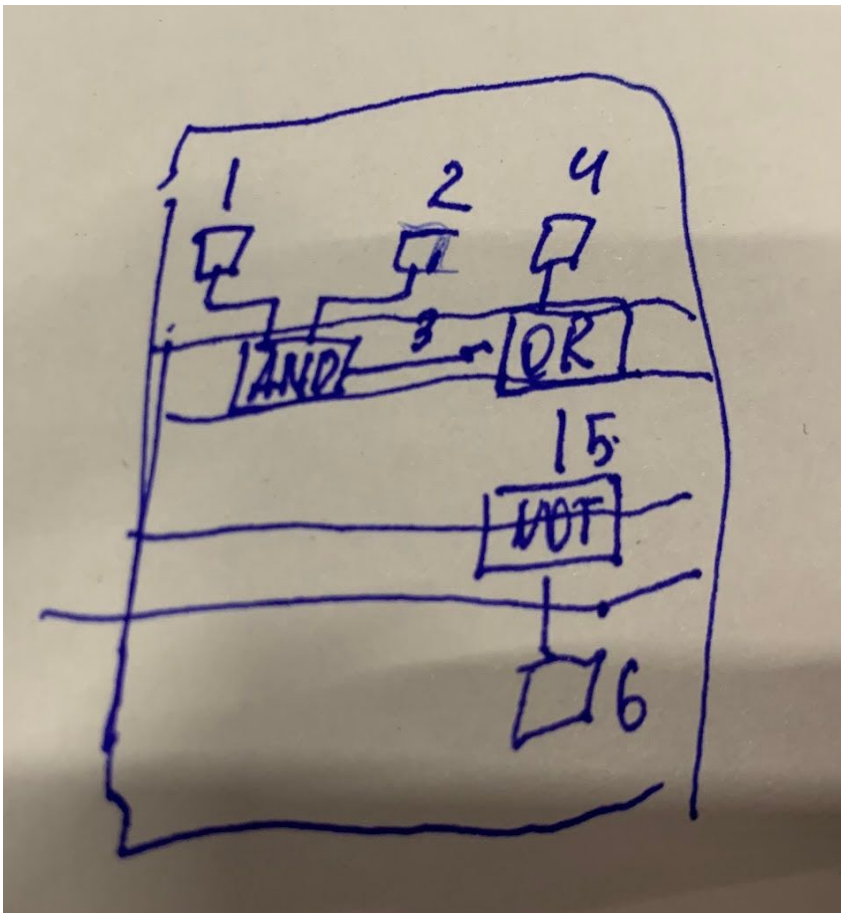
1. The solution will provide a graphical representation of the final placement and routing.
2. Standard cells should be represented as squares of the same size.
3. Standard cells should be placed on the routing channels consequently.
4. Wires on different layers shall be colored in different colors.
5. Wires on the same layers shall be of the same color.

References:

1. Printed circuit board. Retrived online on October 12th, 2019 from: https://en.wikipedia.org/wiki/Printed_circuit_board
2. Printed Circuit Board Terminology. Retrieved online on October 12th, 2019 from: https://www.pcbcart.com/article/content/glossary-of-terms.html
3. Logic gate. retrieved online on October 12th, 2019 from: https://en.wikipedia.org/wiki/Logic_gate
4. Уничтожить монополию Америки в EDA. Иннополис делает первый шаг. Retrieved online on October 13th, 2019 from: https://habr.com/ru/post/469617/?fbclid=IwAR1fG6QSXPRdREk8UdDRRc6OndNHtFgbJnwgVyzJkVpzYFhV7hVb58SJkEI

Appendices

Appendix 1. Graphical representation example 1



Appendix 2. Graphical representation example 2