320MIPS 64bitMPU for space applications

A 320MIPS 64-bit MPU for space applications are being developed under a contract from the Japan Aerospace Exploration Agency (JAXA).

The High-Reliability Engineering & Components Corporation (HIREC) is developing a 320MIPS 64-bit MPU (P/N: HR5000(JAXA2010/101)) for the highly functional space systems of the next generation. HIREC previously developed a 64-bit MPU with a parity check function for space use (P/N NASDA R4901-IDFPR), and it was released in 2001. HR5000 dramatically exceeds NASDA R4901-IDFPR.

High-speed 320MIPS

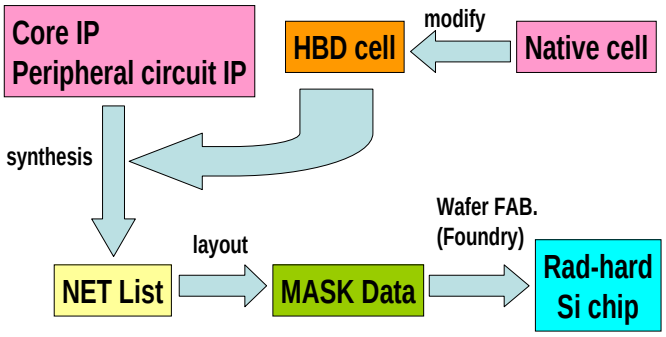
NASDA R4901-IDFPR, the world's only 64-bit MPU for space use, was utilized in Japanese domestic projects including those of JAXA. However, there was some room for improvement in performance, SEU susceptibility and convenience.

HR5000 consists of the MIPS 5Kf™ for the core part and a peripheral circuit. These systems are included on one chip. In order to develop HR5000, HIREC successfully improved a variety of performance parameters compared with NASDA R4901-IDFPR.

Radiation –hardness

Space radiation environments present severe problems in semiconductor devices for space use. Conventional space-use devices are fabricated with special radiation-hardened processes. However, it was not feasible to continue this method because it was difficult to maintain and manage the manufacturing processes. In addition, it will be necessary to utilize state-of-the-art commercial processes to improve the performance of integrated circuits for space use.

HIREC established the Customer-Owned Tooling (COT) procedure for developing advanced LSI circuits for space use. Hardening techniques utilizing the hardness-by-design (HBD) approach are utilized to ameliorate Single-Event Effects (SEE).* Moreover, a radiation-hardened ceramic package is utilized to reduce the influence of Total Ionization Dose (TID).



*Ref.: A. Makihara, et al., "Single-Event Effects in 0.18 um CMOS Commercial Processes", IEEE Trans. Nucl. Sci NS-31, pp 2135-2138, Dec. 2003.

Function Description

Overview

(1)Core: MIPS 5Kf™ 64bitMPU, 200MHz
(2)Peripheral: Eureka Technology ES510 system Controller
(3)PLL: divides INPUT clock to operate Core@200MHz (Max)
(4)Power supply: 1.8V (Core), 3.3V (I/O)
(5)Scan Pass Test
(6)Internal RAM BIST(Built-in self test)

5Kf Core

(1)Floating-point unit (FPU), Translation Lookaside Buffer (TLB)
(2)EJTAG Debug Support
(3)32K bytes instruction & data cache memory with parity check function
(4)Power Down Mode

Peripheral

(1)CPU BUS SLAVE
- Dispatch MPU request to memory controller, PCI, DMAC, TIMER, INTERRUPT CONTROLLER, UART and system control registers.
- Supports separate address and data phases on the EC interface.
- Supports address pipeline by EC interface.
- Supports both single and burst transfer.
- Address translation between the MPU address space and the PCI address space.

(2)Memory Controller
- Receives requests from 3 ports: CPU bus slave, PCI host bridge and DMA controller
- Supports industry standard synchronous burst SRAM, FLASH, ROM and asynchronous SRAM devices.
- Control synchronous burst SRAM @100MHz(Max)
- Automatic issues multiple access to memory device(byte collection) to match data word size of memory devices with user interface data width
- Selectable ECC (enable or disabled)
- Single bit error is correctable, double bit errors are detectable by ECC.

(3)DMA (Direct Memory Access)
- Two DMA channels.
- Supports two types of DMA, Memory to memory and memory to IO data transfer.
- Supports both hardware initiated transfer and software initiated transfer

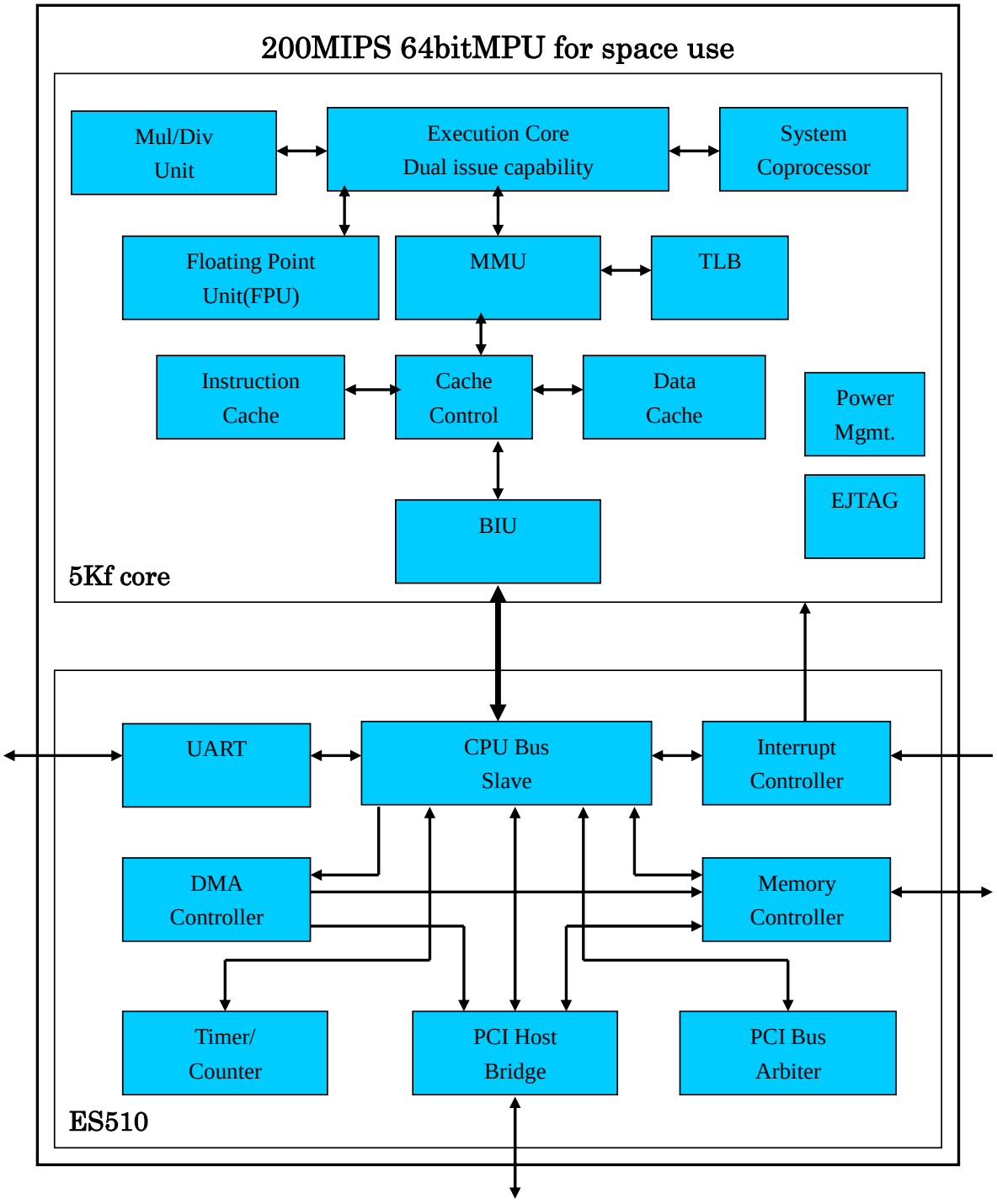
(4)UART (Universal Asynchronous Receiver & Transmitter)
- Independently controlled transmit/receive
- Compatible with 16550 UART.
- Character (16450) and FIFO (16550) mode operations.
- 16-byte FIFO for transmitter and receiver reduces the number of interrupt to the CPU.
- Holding and shift register in non-FIFO mode eliminates the need for precise synchronization between the CPU and UART.
- Programmable baud generator divides input clock by 2 to (2^{16}-1) and generates the 16X clock.

(5)TIMER/COUNTER
- 32-bit up counter x 2 channels
- devisable 1/2～1/256

(6)INTERRUPT CONTROLLER
- Supports 9 kinds of internal interrupts from internal circuit and 6 external interrupt input signals.
- Interrupt detection mode can be selected from edge or level for each external interrupt.
- 8 level of interrupt priority setting for each interrupt input.

(7)INTERFACE
- Fully supports PCI specification 2.2 protocol.
- Both PCI address and data are 32-bits.
- Master receives requests from CPU interface.

Function Block Diagram



ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{DDI}	1.8±0.1 (CORE)	Vdc
	V_{DDE}	3.3±0.3 (I/O)	Vdc
I/O Input Voltage	V_{IO}	−0.3～V_{DDE}+0.3	Vdc
I/O Output Voltage	V_{OL}	0～0.2	Vdc
	V_{OH}	V_{DDE}−0.2～V_{DDE}	Vdc
Maximum Power Dissipation	P_{Dmax}	4(low Power type) 6(High Speed type)	W
Operating Frequency Range	F	20～200	MHz
Operating Temperature Range	Tc	−40～+85	℃
Storage Temperature Range	Tstg	−55～+125	℃

Package feature

(1)304pin Ceramic QFP

(2)Weight: 40g (except Tie-bar)

(3)Dimension(W×D×H) :47mm×47mm×3.25mm(ceramic body)

78mm×78mm×3.25mm(including Tie-bar)

Development Environment

Item	Environment	Company
Compiler	C++,C,Asembla	GNU
OS	uITRON	eSOL
ICE(In-circuit emulator)	AdvicePlus	YDC

HIREC

High-Reliability Engineering & Components Corporation