



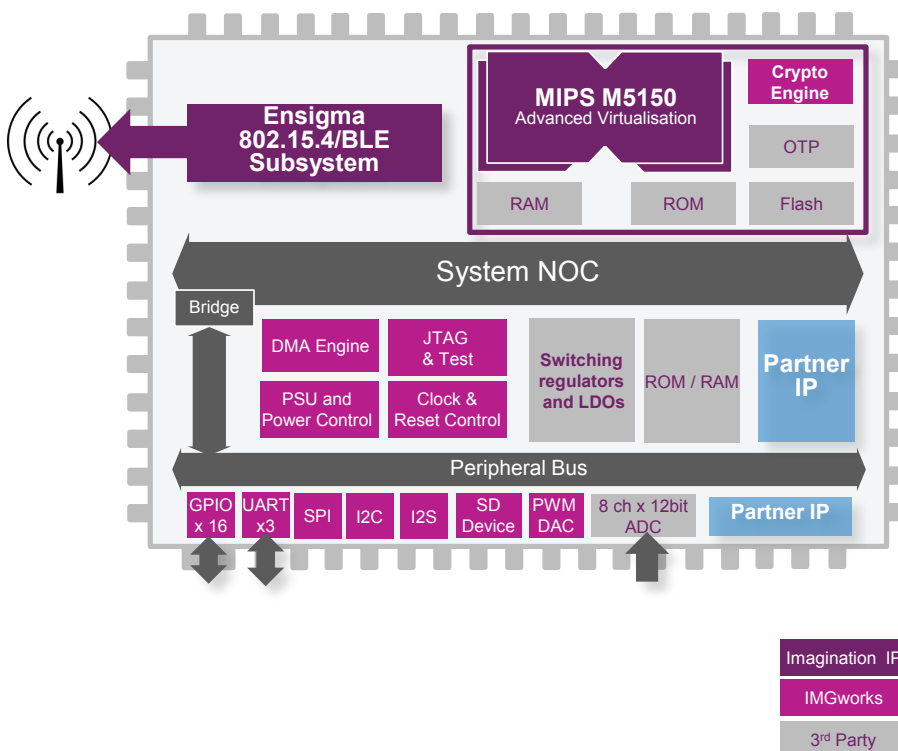
# Oberon – Integrated Intelligent Sensor

## Wireless MCU Solution for the Internet of Things

Oberon is an integrated microcontroller which includes wireless connectivity, security, and power management in a small footprint device that is ideal for M2M (machine-to-machine) communications via local networks or the Cloud.

Support for M2M communications via Bluetooth and 802.15.4 is included and Oberon provides a robust, secure environment using Imagination's Omnishield™ security technology. The M5150 processor features hardware virtualization, secure boot, embedded flash, and integrated boot ROM within the encryption boundary of the device, providing high levels of security for the data and software running on the device.

An SDK and development board for software development are included with Oberon. The SDK supports 6LowPAN and THREAD which are important stack components for the Internet of Things. The SDK also includes the FlowM2M™ client service for direct connection Imagination's cloud platform, FlowCloud™.



Oberon Integrated Intelligent Sensor block diagram

## Features

Embedded MIPS M5150 CPU with virtualization

Secure features include:

- Hardware assisted virtualization
- Secure boot
- Public Key Authentication
- Hardware encryption

Integrated 802.15.4/BLE including baseband and transceiver

Integrated flash to 1MB

Integrated retention SRAM to 64 KB

Integrated 8 channel 12-bit A/D

Integrated thermal sensor

SDIO slave

3 x SPI interface

3 x UART

2 x I<sup>2</sup>S receiver for microphone or audio input

I<sup>2</sup>S transmitter for interface to speaker

Integrated switching and LDO regulators

## Benefits

Complete single chip M2M IoT device

IoT software stack for cloud connectivity

Designed for secure applications

## Applications

Smart metering

Intelligent Sensor controller

Industrial IoT

# Oberon Specification

## CPU Subsystem

Single core MIPS M5150 embedded microcontroller with built in virtualization. The MIPS M5150 CPU includes an integrated DSP pipeline.

The CPU subsystem includes 32K I\$ and D\$ L1 cache

Integrated secure OTP for secure key

Secure boot and integrated boot ROM

SPI interface inside the secure encryption boundary to connect to external SPI flash

Integrated Private key accelerator for session authentication

Integrated CRDMA to support AES, DES, 3DES encryption

CPU is optimized for low power and active power dissipation is 3.0 mW @ 100MHz.

## BTLE / 802.15.4 Wireless Connectivity

Integrated baseband controller, AFE and 2.4 GHz transceiver

Integrated power amp to +3 dBm.

## Peripheral Subsystem

SD slave

3 x UART

3 x SPI interface

Up to 16 bits programmable GPIO

3 x I<sup>2</sup>S interface to support wireless audio applications.

Dual I<sup>2</sup>C interface

## Analog Subsystem

8-channel 12-bit A/D converter @ 1 MHz.

## Power Management

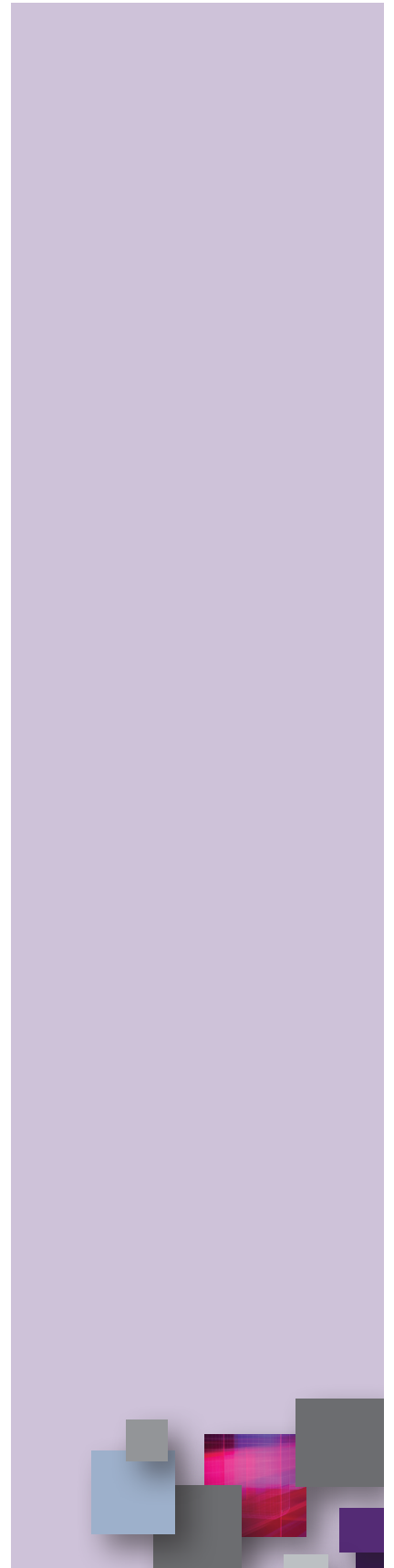
Integrated power management provides dynamic voltage and frequency scaling to minimize power consumption

External inputs provided to wake up or put device to sleep mode

Integrated switching and LDO regulators that permit chip to be powered from only 3.3 V source

## Package

QFN package from 36 to 100 pins



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