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GODSON-3 EMULATES X86

New MIPS-Compatible Chinese Processor Has Extensions for x86 Translation

By Tom R. Halfhill {11/3/08-01}

The hottest presentation at the recent Hot Chips Symposium at Stanford University was the world's first look at the Godson-3, the latest generation of China's most powerful microprocessor family. It was the first time a Chinese CPU architect visited the U.S. to lift the bamboo curtain on a home-grown Chinese processor at a major technical conference. Journalists from industry publications as well as from mainstream media eagerly joined the usual Hot Chips audience of engineers for a peek at the new design.

There was much to admire. The Godson-3, also known as the Loongson-3, is the first multicore member of this seven-year-old Chinese microprocessor family. The initial Godson-3, taping out this year, integrates four MIPS-compatible 64-bit processor cores in a crossbar network. This quad-core block is scalable, so future implementations may have dozens of cores. (Smaller implementations are planned, too.) The first chips will be fabricated in 65nm CMOS, and clock speeds are expected to hit 1.0GHz.

Equally interesting is an optional on-chip coprocessor for signal processing and high-performance floating-point math. The initial quad-core Godson-3 won't have this coprocessor, but a second implementation, scheduled for tapeout in 2009, will have four of them, along with four of the MIPS-compatible cores. By leveraging this extra horsepower, the Chinese hope to build a supercomputer within two years that executes one petaflops (one quadrillion floating-point operations per second). That performance would match the fastest supercomputer in the world today.

PHOTO COURTESY OF HOT CHIPS SYMPOSIUM

The Godson-3 was presented at the Hot Chips Symposium by Zhiwei Xu, a professor at the Institute of Computing Technology, Chinese Academy of Sciences.

As if those revelations aren't enough, the Godson-3 has another startling feature: more than 200 new instructions and other modifications that accelerate x86-to-MIPS dynamic binary translation. In other words, the Godson-3 applies hardware optimization to x86 emulation, much as Transmeta did with its Crusoe and Efficeon microprocessors.

That feature raised a few eyebrows. Godson processors are designed at the Institute for Computing Technology (ICT), part of the Chinese Academy of Sciences in Beijing. ICT does not have a license for either the MIPS or x86 architectures. Last year, ICT resolved an intellectual-property dispute with MIPS Technologies by partnering with STMicroelectronics, a MIPS licensee. But do the x86-like extensions risk another conflict—this time with Intel, and perhaps with Transmeta as well?

Godson-3 Isn't an x86 Clone

At *Microprocessor Report*, we aren't patent attorneys, but our initial analysis is that the Godson-3's extensions probably don't tread on intellectual property owned by Intel (the inventor of the x86 architecture) or Transmeta (whose hardware-assisted "code morphing software" advanced the art of x86 emulation). The Godson-3 doesn't appear to go as far toward x86 compatibility as Transmeta's processors did, and Transmeta had no legal

problems with Intel for almost seven years. Intel and Transmeta didn't clash until 2006, when Transmeta filed a patent-infringement lawsuit against Intel, prompting Intel to respond with a countersuit. Both suits were quickly settled out of court, largely in Transmeta's favor. (See *MPR 12/26/07-01*, "Transmeta's Second Life.")

An important difference between Transmeta's discontinued processors and the Godson-3 is that the Chinese don't claim to be making x86-compatible chips. Like earlier Godson processors, the Godson-3 is designed to natively run MIPS-compatible software. Hardware-assisted x86 emulation is a last resort for software unavailable on MIPS. (And the Chinese are undertaking a major effort to port more software to MIPS.)

In contrast, Transmeta marketed its Crusoe and Efficeon chips as fully compatible with the x86 and never opened their native VLIW architectures to outside software developers. Also, Transmeta promised competitive x86 performance, whereas the Chinese are making no such claims for the Godson-3.

Nevertheless, the Godson-3's extensions almost certainly have Intel and Transmeta watching with renewed interest. Neither Intel nor Transmeta will comment publicly, but Intel sent a patent attorney to observe the Godson-3 presentation at Hot Chips. If there's a more heavily patented CPU architecture than the x86, we don't know about it, so there's always a possibility the extensions will step on someone's toes.

Despite those concerns, *MPR* considers the Godson-3 a significant improvement over the Godson-2 series. It moves Chinese microprocessor technology closer to the state of the art, as practiced by the likes of AMD, IBM, Intel, and Sun Microsystems. The Godson-3 will advance China's quest for greater technology independence—a vital part of the nation's long-term economic strategy. (See *MPR 6/26/06-02*, "China's Microprocessor Dilemma," and *MPR 7/25/05-01*, "China's Emerging Microprocessors.")

Chinese Chips for China

Much as the U.S. yearns to be energy independent, China yearns to be technology independent. For everyone, computing has become a fundamental resource, as vital to national security and economic prosperity as oil. The world's most populous nation doesn't want to depend on foreign microprocessors for all its computing needs. Also, export restrictions prevent U.S. companies from selling their best technology to China. That's why Godson development is partly funded by the Chinese government, as well as by private investors. It's a crucial part of China's long-term projects for developing indigenous technology that's competitive with foreign technology.

For now, Godson processors are intended mainly for the Chinese domestic market. ICT launched the Godson project in 2001 and finished the 32-bit Godson-1 in 2002. Next came the 64-bit Godson-2 series, including the Godson-2B in 2003, Godson-2C in 2004, Godson-2E in 2006, and Godson-2F in 2008. The Godson-2G is taping out now, and a Godson-2H chip that integrates a GPU, north bridge, and south bridge is scheduled for tapeout next year. Godson is ICT's name for this microprocessor family. Commercially, the chips are usually marketed under the names Loongson or Dragon.

Most Godson processors are largely compatible with the MIPS-III and MIPS-IV instruction-set architectures, omitting a few features patented by MIPS. Godson-2 processors are found in Chinese embedded systems, low-cost Linux PCs, Linux servers, and a few Western products. Examples of netbook PCs with Godson processors include the EMTEC Gdium, the HiVision MiniNote (a $98 Linux netbook), and the Lemote Fuloong Mini PC. Outside China, there's the Maplin Minibook, an ultramobile PC with a seven-inch screen that retails in the U.K. for £170.

In a deal concluded with MIPS and ICT last year, STMicroelectronics is manufacturing some Godson chips and may fabricate the Godson-3 as well. In contrast with the "MIPS-like" cores in earlier Godson chips, the GS464 core in late-model Godson-2 chips and the Godson-3 is legally compatible with the MIPS64 architecture, according to MIPS. Assuming the Godson-3 passes final verification tests, it can be promoted as "MIPS Based" and "MIPS Verified"—labels trademarked by MIPS. (See *MPR 4/23/07-01*, "Embedded Systems Conference Highlights.")

Because Godson processors are intended mainly for Chinese consumption, ICT designs them to meet the broad requirements of the Chinese domestic market, not necessarily to compete with microprocessors in other parts of the world. Godson-3 processors will find their way into everything from embedded systems to servers, with special emphasis on affordable Linux PCs for Chinese homes, businesses, and schools.

Initial implementations of the Godson-3 reach toward the higher end of the performance spectrum, probably as proof-of-concept for larger designs in the future. (Scaling down is easier than scaling up.) As mentioned above, the first Godson-3 will have four GS464 cores, followed by a similar design that adds four coprocessors. Both chips will be suitable for Linux workstations and servers. Single-core implementations will be suitable for embedded systems—and perhaps for low-cost Linux PCs. Further forward, the quad-core cluster could be the foundation for massively parallel computers with dozens or hundreds of cores. Those larger implementations could power the supercomputer that China hopes to build by 2010.

A Powerful MIPS-Compatible Core

At the heart of the Godson-3 is the GS464 processor core, one of the most powerful MIPS-compatible cores ever conceived. Although ICT has improved the GS464 for the Godson-3, it is appearing first in some late-model Godson-2 chips, such as the Godson-2F. The GS464 is a 64-bit core with four-way superscalar execution, out-of-order instruction processing, dynamic branch prediction, and speculative execution.

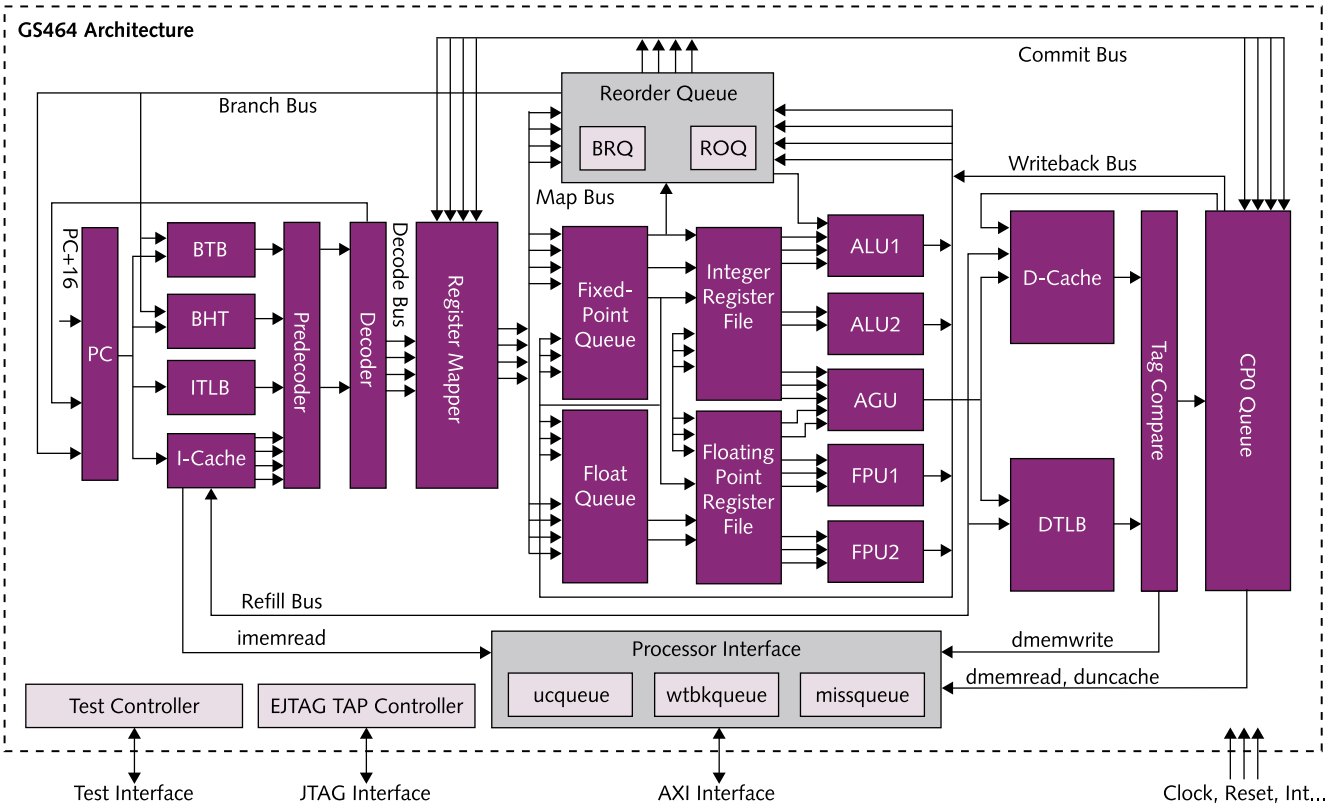

Figure 1. Block diagram of the GS464 processor core. Although it's based on the 64-bit processor core in earlier Godson-2 chips, the GS464 is now fully compatible with the MIPS64 instruction-set architecture. Four-way superscalar pipelining with out-of-order instruction handling and speculative execution make it one of the most powerful MIPS-compatible cores yet seen. The translation lookaside buffer (TLB) has 64 entries and is fully associative. It is supplemented by a 16-entry instruction TLB (iTLB). The L1 instruction cache has parity checking, and the L1 data cache has ECC. The 128-bit system interface is compatible with the AMBA 3.0 AXI specification, a feature normally seen in ARM processors.

Function units include two ALUs, two FPUs, and one address-generation unit (AGU). The fully pipelined 64-bit FPUs can handle double-precision floating-point instructions or pairs of single-precision instructions, as well as multiply-accumulate (MAC) operations.

To support register renaming for out-of-order execution and speculation, the GS464 processor core has 64 integer registers and 64 floating-point registers—twice the complement of the standard MIPS architecture. The GS464 retires results in original program order from a 64-entry reorder queue. For branch prediction, the GS464 has an 8,192-entry branch-history table, a nine-bit global-history register, a 16-entry branch-target buffer, and a four-entry return-address stack. The GS464 can speculatively execute loads and stores out of order without blocking the caches, thanks to memory disambiguation and a 24-entry memory-access queue implemented as content-addressable memory (CAM). Figure 1 is a block diagram of the GS464.

The GS464 has 64KB L1 instruction and data caches, both four-way set-associative. The initial quad-core Godson-3 will have four L2 caches, each 1MB, attached to the same crossbar network as the four processors. The 8 × 8 crossbar connects the processors with the L2 caches and will also connect with neighboring quad-core clusters in larger Godson designs. All four cores in a cluster can share the L2 caches. A directory-based cache-coherency protocol allows global cache access.

Programmers can use the L2 caches as software-managed scratchpads, too. The DMA engine can prefetch data into an L2 cache and perform a few tricks, such as transposing the data elements of a matrix during a memory transfer. The GS464 supports 48-bit physical and virtual memory addressing. Figure 2 illustrates the configuration of a basic quad-core GS464 cluster.

The quad-core cluster is a potential building block for constructing larger multicore designs and massively parallel designs. Figure 3 illustrates a possible implementation built around two clusters. Clusters linked in this fashion can share data over their 16-bit HyperTransport 1.0 interfaces, which can also function as eight-bit interfaces in larger clusters. These clusters can maintain cache coherency among their L2 caches, even across multiple chips.

Further down the road, ICT could organize several clusters into a larger mesh network. Even the smallest of these

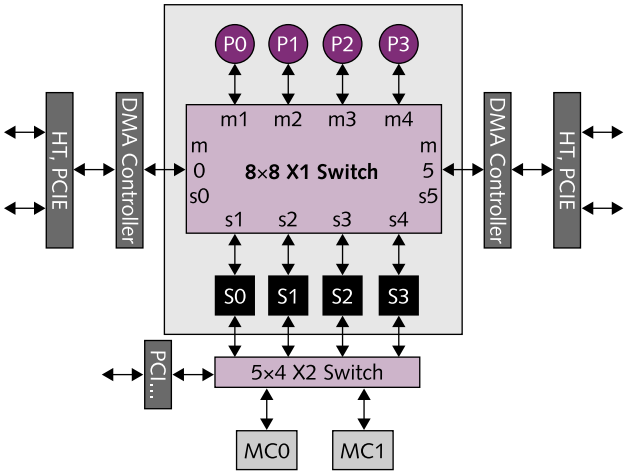

Figure 2. Cluster of four GS464 processor cores sharing four coherent L2 caches. The 8 × 8 crossbar network provides direct connections among all the cores and L2 caches. In addition, the crossbar can connect a quad-core cluster with neighboring clusters in the north, south, east, and west directions. The initial implementation of the Godson-3 has only one cluster, so those connections are unused, but future designs could support massively parallel processing in a large on-chip fabric.

possible designs would fit the vague definition of a "many-core" microprocessor. With 16 or more clusters—that is, 64 or more GS464 cores—a future implementation could lay claim to being massively parallel. Figure 4 illustrates such a design.

At Hot Chips, the Godson-3 presentation confused some audience members by describing the future quad-core implementation with four coprocessors as an "eight-core" microprocessor. This description is technically correct—it's an eight-core heterogeneous multicore processor. Similarly, *MPR* considers IBM's Cell Broadband Engine to be a multicore chip, even though it has only one Power Architecture core. The other eight cores in a Cell BE chip are the Synergistic Processor Elements (SPE), which are SIMD coprocessors, somewhat like the coprocessors planned for future Godson-3 chips. (See *MPR 2/14/05-01*, "Cell Moves Into the Limelight.")

Likewise, an eight-core Godson-3 chip that integrates four GS464 cores with four coprocessors may be considered a heterogeneous eight-core microprocessor. Confusion over this point has two sources. First, the initial Godson-3 chip is a homogeneous quad-core design without coprocessors, implying homogeneity in future designs. Actually, the Godson-3 architecture supports either homogeneous or heterogeneous implementations. The second source of confusion is that, so far, all the mainstream multicore processors from AMD and Intel are homogeneous, leading some observers (usually not engineers) to assume that all multicore processors are homogeneous.

New Coprocessors Add Horsepower

The Godson-3's coprocessors are themselves a source of minor confusion. Although they provide additional floating-point horsepower, as well as signal-processing capabilities, they are unlike the usual FPUs attached to most modern CPUs. Indeed, the GS464 core already has two MIPS-compatible 64-bit FPUs.

The new coprocessors are supplemental engines, more like the SPEs in IBM's Cell. They are not MIPS-compatible cores. They have a proprietary architecture, as yet undisclosed, programmable in low-level microcode. Most programmers will probably access the coprocessors through a high-level application programming interface (API) that encapsulates common functions. A well-known example of a microcode-programmable coprocessor used in this manner is the QUICC Engine in Freescale PowerQUICC processors.

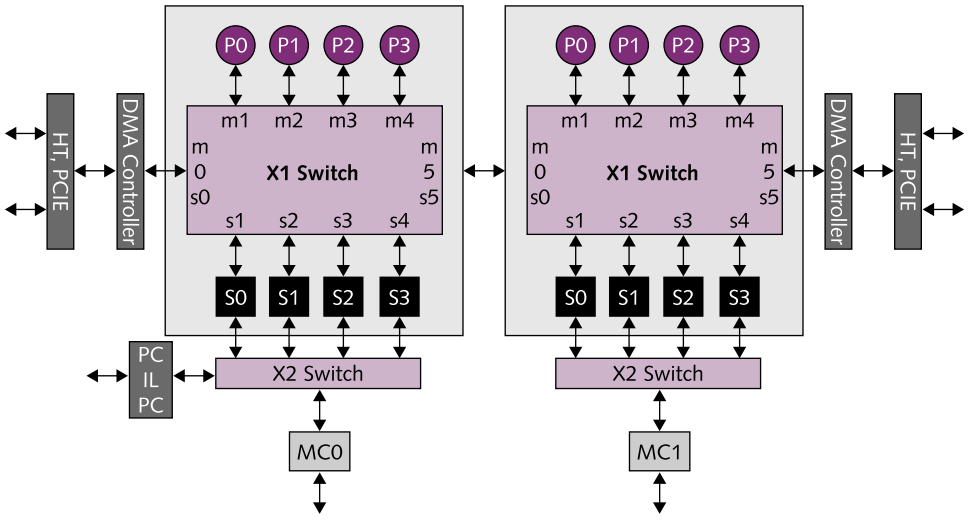

Figure 3. Two GS464 clusters linked together, forming an eight-core microprocessor (not counting coprocessors). This design is a theoretical but likely extension of the initial quad-core Godson-3.

ICT refers to the Godson-3 coprocessor as a "GStera multipurpose core." (GS stands for Godson, and "tera" refers to teraflops.) In contrast, ICT refers to the MIPS-compatible core as the "GS464 general-purpose core." The distinction between general-purpose and multipurpose is subtle but important. Whereas the general-purpose GS464 can do anything, the multipurpose GStera can do multiple things—but it's not a special-purpose core in the same sense as a cryptography engine, regular-expression engine, or some other dedicated hardware block. (Congratulations to the anonymous Chinese translator who preserved this distinction.)

According to ICT, the GStera coprocessor is intended for "LINPACK, biology computation, and signal processing." LINPACK, of course, is a floating-point benchmark suite, often used to measure the performance of supercomputers. "Biology computation" undoubtedly refers to protein folding and similar tasks important in medical research. Generally, scientific computing of this sort is a job for supercomputers, although it can also run effectively on GPUs and on numerous smaller computers distributed across a network. An example of the latter is Stanford University's Folding@home project, which runs a small protein-folding program on thousands of idle PCs and game consoles attached to the Internet.

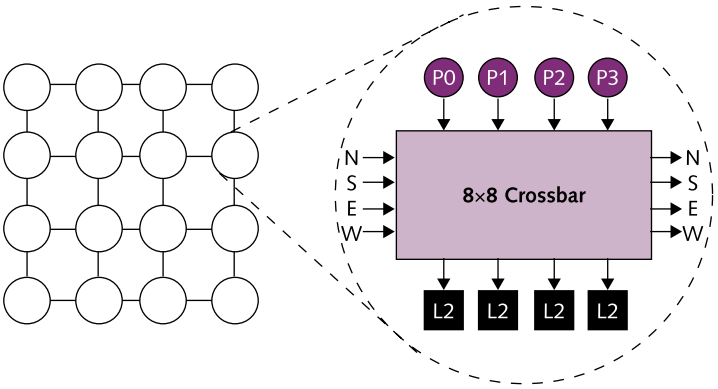

Figure 4. A massively parallel implementation of the Godson-3 could populate the on-chip mesh network with 16 or more quad-core clusters. This figure is based on a slide shown at the Hot Chips Symposium by one of the Godson-3 designers, so it's not a far-fetched speculation. An implementation this large and powerful is probably intended for a future Chinese supercomputer.

Building a Supercomputer by 2010

Figure 5 is a block diagram of the GStera coprocessor. Each engine has eight function units, each with its own register file. These files are huge—1,024 registers, 64 bits wide. (Their layouts are manually optimized, not left to the mercies of automated place-and-route tools.) Each register file has four read ports and four write ports. An AXI controller with DMA connects to the chip's global AXI interface, so the GStera coprocessors can fetch data from memory without bothering the CPUs. Thanks to crossbar connections, the function units can also communicate with other GStera coprocessors and with GS464 cores in the same quad-core cluster.

A small microcontroller supervises each GStera coprocessor. ICT hasn't disclosed details about this controller, but it probably executes the microcode that drives the function units. This arrangement suggests that the coprocessors enjoy a higher level of autonomy than conventional FPUs. The DMA controller in the AXI interface is another indication that the GStera coprocessors are a cut above the typical FPU. Usually, FPUs fetch their instructions and data through the same I/O interface as the ALUs.

Performance data for the coprocessors is sparse at this time. ICT says each function unit can execute 8 or 16 MAC instructions simultaneously—probably one 64-bit MAC or two 32-bit MACs. At 1.0GHz, maximum theoretical throughput is 16 gigaflops (16 billion floating-point operations per second). Using the coprocessors alone, the future Godson-3 design that integrates four GS464 cores with four GStera coprocessors could reach 64 gigaflops. The two MIPS-compatible FPUs in each GS464 core can execute four gigaflops, so total performance would be 80 gigaflops per

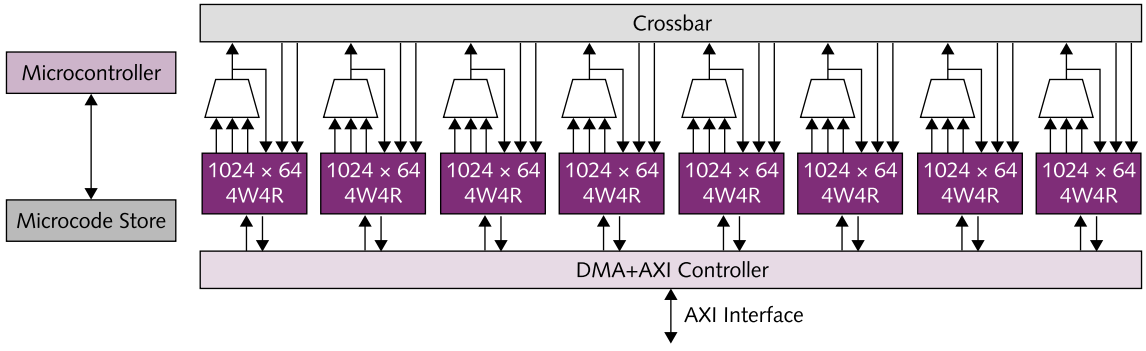

Figure 5. GStera coprocessor block diagram. Each coprocessor has eight function units with large register files, four read ports, and four write ports. Dedicated interfaces to the AXI interface and crossbar network allow each coprocessor to communicate with other coprocessors and GS464 cores.

cluster. The 16-cluster massively parallel design envisioned in Figure 4 would exceed 1.2 teraflops (1.2 trillion floating-point operations per second).

ICT speaks of "teraflops for the masses," suggesting that 16-cluster chips will be affordable for medium-size number-crunching machines. So-called "desktop supercomputing" is the latest craze. Although they aren't world-class supercomputers, these small, affordable systems can be as powerful as the supercomputers of the 1990s. Often, they are built with GPUs from ATI or Nvidia, or with specialized processors, such as IBM's Cell or ClearSpeed's floating-point coprocessors. Intel's future Larrabee chips will be contenders in this fast-growing field, too. (See *MPR 9/29/08-01*, "Intel's Larrabee Redefines GPUs," *MPR 1/28/08-01*, "Parallel Processing With CUDA," and *MPR 2/9/04-15*, "Extreme CPUs Defy Conventions.")

But ICT has bigger ambitions than desktop supercomputing. By 2010, ICT hopes to build a world-class supercomputer for a "national strategy application." This machine is expected to execute at least one petaflops (one quadrillion floating-point operations per second). To reach that goal with the Godson-3, the supercomputer needs at least 782 of the 16-cluster chips, by our reckoning.

That's a lot of chips, but by no means unrealistic for a true supercomputer. IBM's BlueGene/L supercomputer, built at Lawrence Livermore National Laboratory in 2004, has 65,536 Power processor chips, each with two cores. Rated by LINPACK at 478.2 teraflops, BlueGene/L reigned as the world's fastest supercomputer until last June. Then it was surpassed by IBM's new Roadrunner supercomputer at Los Alamos National Laboratory. According to Top500.org, a supercomputer-ranking site, Roadrunner was the first computer to break the petaflops barrier. (See *MPR 10/11/04-01*, "IBM Makes Designer Genes.")

It's highly unlikely that a Chinese supercomputer based on the Godson-3 will surpass the world's fastest computers by 2010. However, the Chinese have a shot at improving their position in the Top 500—and with the Godson-3, the machine could boast Chinese technology. Right now, the fastest supercomputer in China ranks number 111. It's an IBM BladeCenter cluster with 2,048 Intel Xeon dual-core processors. China has only 12 supercomputers in the Top 500, none built with Chinese processors.

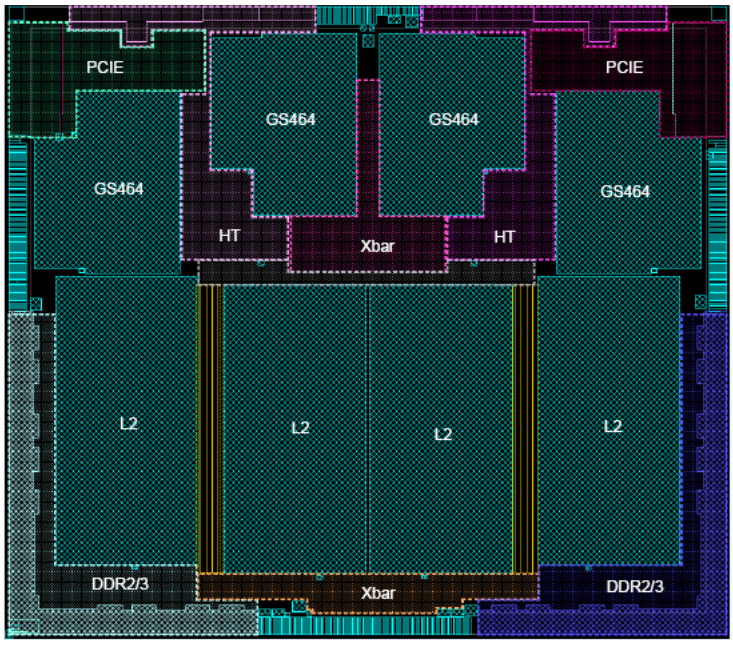

Figure 6. Quad-core Godson-3 layout. ICT is taping out this design by the end of this year. Die area is 174mm^2 in a 65nm CMOS process with seven layers of metal. The large L2 caches (1MB each) dominating the layout are no surprise, but the arrangement of the four GS464 processor cores is somewhat unusual. Normally, one would expect four cores linked by a crossbar network to be arranged in a pattern more nearly square, instead of in a row. Communications between the two outer cores will suffer longer wire delays than communications between the inner cores.

Optimizations for Power Consumption

Smaller versions of the Godson-3 are intended for embedded systems, so low power consumption is another important objective. The first Godson-3 chips will be fabricated in a 65nm CMOS process that mixes low-power and general-purpose features.

Reducing power consumption with fabrication technology is vital, because the Godson-3 is largely a synthesized cell-based design with an automated layout. ICT has manually optimized only the most critical paths and blocks. For instance, the register files are custom designs, as are the TLB, PLL, and HyperTransport physical-layer (PHY) controller. Hand-tooled clock gating reduces power consumption in major blocks, including the CPU cores, HyperTransport controller, PCI Express controller, and DDR2/DDR3 memory controller. As is customary in optimized designs, some circuits use high-threshold transistors for low static leakage, whereas others use low-threshold transistors for faster switching.

The Godson-3 will be capable of scaling its core voltage and clock frequency up or down to save power, but ICT hasn't released details about its implementation of this widespread technology. An on-chip temperature sensor can automatically throttle the processor if it runs too hot—another common feature in modern microprocessors.

Thanks to all these efforts, ICT says the initial quad-core Godson-3 will dissipate only 5–10W at 1.0GHz. That estimate appears to be a "typical" rating, not the maximum rating that system designers need to anticipate cooling requirements. The eight-core Godson-3 scheduled for tapeout in 2009—four GS464 CPU cores plus four GStera coprocessors—is expected to dissipate 20W at 1.0GHz. Again, that estimate appears to be a "typical" specification.

STMicroelectronics has fabricated a test chip in 65nm CMOS. However, it lacks many features of the final design, including the GS464 cores, so it's not indicative of production silicon. ICT says the final production chip will measure 14.2mm × 12.2mm. The test chip allows engineers to verify operation of the hand-optimized register files, CAMs, and HyperTransport controller. Instead of reproducing a die photo of the chopped-down test chip, we show the layout of the full quad-core design in Figure 6.

Extensions Accelerate x86 Emulation

ICT refers to its x86 emulation technology as XBAR, which stands for "x86 Binary-translation Acceleration on RISC." (Not to be confused with the crossbar network that links multiple cores together, which is sometimes abbreviated as XBAR, too.) XBAR extensions include more than 200 new instructions beyond the standard MIPS64 instruction set, plus additional modifications.

In general, XBAR extensions try to resolve the numerous differences between a CISC architecture designed in the 1970s and a RISC architecture designed in the 1980s. Without XBAR, a MIPS-compatible processor might need 40 or more RISC instructions to emulate a complex x86 instruction. XBAR reduces that ratio, sometimes achieving one-to-one correspondence.

As Figure 7 shows, XBAR supports system-level and processor-level virtual machines on Linux. To emulate the x86 at the processor level, ICT is extending the free QEMU dynamic binary translator developed by French programmer Fabrice Bellard. According to ICT, the latest tests indicate the Godson-3 will run x86 code about half as fast as the same code natively compiled for MIPS. ICT hopes to reach 80% native MIPS performance. The trade-off is that XBAR adds about 5% more die area to the Godson-3. If XBAR works as well as ICT hopes it will, the extra silicon cost and power consumption will be small prices to pay.

A good example of the Godson-3's hardware support for x86 emulation is the EFLAGS status register. EFLAGS is a 32-bit register that stores information about the current status of a 32-bit x86 processor. Earlier x86 processors used the 16-bit FLAGS register for this purpose. The FLAGS register was extended to 32 bits (EFLAGS), starting with the Intel 386, and later to 64 bits (RFLAGS) in the x86-64 architecture. (The Godson-3 supports 32-bit x86 emulation.) In the x86, most integer arithmetic instructions alter the status flags in this register. Subsequent branch instructions read the flags to determine the direction in which to jump. In the MIPS architecture, branch instructions read values in general-purpose registers to determine in which direction to jump.

Emulating EFLAGS with standard MIPS instructions can be costly. ICT gives the example of an x86 subtraction instruction (SUB ECX, EDX) followed by a jump-if-equal (JE) instruction. While performing a simple register-to-register subtraction, SUB alters four status bits in the EFLAGS register: SF (sign flag), ZF (zero flag), OF (overflow flag), and CF (carry flag). Translating this behavior into MIPS instructions is a painful exercise requiring 41 instructions. With XBAR in the Godson-3, the same translation requires only three or four instructions.

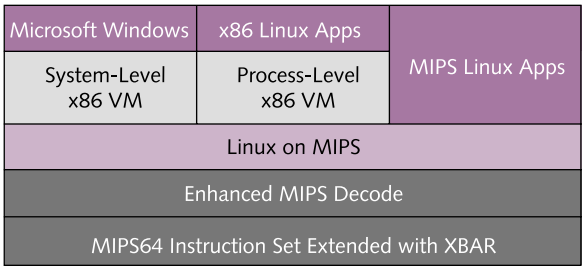

Figure 7. Two examples of x86 virtual machines running atop a MIPS version of Linux on the Godson-3. The Godson-3's x86 acceleration technology is called XBAR (x86 Binary-translation Acceleration on RISC). It supports processor-level and system-level virtual machines.

For the most commonly used x86 instructions, XBAR defines new instructions that perform the same operations and set the same status bits in the EFLAGS register. These new instructions are one-to-one replacements for x86 instructions. For instance, the new XBAR counterpart of SUB is X86SUB, and the new XBAR counterpart of JE is X86JE. For less common x86 instructions, XBAR defines a new SETFLAG instruction that sets the status bits as a separate operation.

Emulating FP and Multimedia Instructions

Another characteristic of the x86 architecture is 80-bit extended-precision floating-point math. MIPS and almost all other CPU architectures use 64-bit double-precision math. Not many real-world x86 programs use 80-bit operations, but emulators must support it. Another oddity is that the eight floating-point registers in an x86 (actually x87) FPU are organized as a stack, not as a flat register file. MIPS and most other CPU architectures use flat register addressing.

Normally, translating between 64- and 80-bit numbers requires about 40 standard MIPS instructions. XBAR defines one new instruction (CVT) that converts an 80-bit number stored in two 64-bit registers into a 64-bit number that fits into one register. Two instances of the CVT instruction with different operand fields can reverse that conversion. Also, XBAR organizes the floating-point registers as a flat file, not as a stack. A register-renaming scheme preserves compatibility for x86 stack operations. This scheme saves about ten MIPS instructions when translating each x86 floating-point instruction.

Multimedia extensions to the x86 are yet another challenge. The Godson-3 supports MMX, SSE, and SSE2. Apparently, it does not support SSE3, Supplemental SSE3 (SSSE3), or the latest SSE4.1. All x86 multimedia instructions execute in the GS464 core's FPUs, even when those instructions use integers. The reason for using FPUs is that they're better prepared to handle the various datatypes that x86 multimedia

instructions manipulate. Some x86 SIMD instructions operate on four 16-bit integers or eight 8-bit integers at a time. Standard MIPS floating-point instructions already use a five-bit field to define different datatypes: single-precision floating point, double-precision floating point, paired single-precision floating point, fixed-point words, and fixed-point longwords. XBAR extends that field to define the additional SIMD datatypes that x86 processors use.

The MIPS architecture supports unaligned loads and stores, a valuable feature when manipulating odd-sized multimedia datatypes. However, standard MIPS instructions can load or store unaligned data in only the general-purpose integer registers, not in the floating-point registers. To reduce traffic between the two register files, the GS464 core can assign floating-point registers as targets for unaligned load and store instructions. This modification further improves x86 multimedia translation.

Memory addressing raises other issues when emulating the x86. Older CISC architectures have addressing modes that newer RISC architectures discarded. The GS464 revives some of those modes, including one that adds a displacement to a base address with an index. To emulate x86 segmented-memory addressing, the GS464 can raise an exception if a load or store instruction exceeds certain bounds defined by a register.

As a substitute for the 8- and 16-bit arithmetic operations in the x86, the GS464 can insert or extract partial values in its 64-bit registers. Partial values can be 8, 16, or 32 bits long. New instructions can insert or extract these values at any location in a register, padding unused bits with zeroes.

Further Optimizations for x86 Translation

Dynamic binary translators usually cache frequently executed blocks of code in a special region of memory. When the translator encounters the same block of code in the emulated program, it can fetch the already-translated code from the cache instead of translating it again. The code-morphing software for Transmeta's Crusoe and Efficeon processors reserved several megabytes of main memory for this purpose. It's not clear whether the Godson-3 uses this technique. However, it does keep some code in the on-chip L2 cache, which is 1MB per core in the initial quad-core version of the microprocessor.

One special memory that the Godson-3 does have is a lookup table for indirect branches. Dynamically translating an x86 indirect-branch instruction into a native MIPS branch instruction is inefficient. The Godson-3 has a 64-entry table of branch addresses. New table-lookup instructions allow the translator to rapidly find the indirect address and final address of a branch. The lookup table is implemented as a CAM, much like the TLB.

ICT says it is improving the QEMU open-source x86 dynamic binary translator, mainly by writing a new interpreter and translator for the Godson-3. ICT's virtual-machine monitor can identify critical sections of x86 code and help the translator apply various optimizations, depending on the perceived importance of the code. Java just-in-time compilers commonly use the same techniques.

Transmeta applied these optimizations and more in its Crusoe and Efficeon processors, yet their performance generally lagged behind Intel's x86 processors. However, apples-to-apples comparisons were difficult. For one thing, Transmeta emphasized low power consumption over maximum throughput. For another, the caching behavior of Transmeta's code-morphing software could fool benchmark programs that use loops to measure performance. (See *MPR 2/14/2000-01*, "Transmeta Breaks x86 Low-Power Barrier.")

ICT has already been testing x86 performance on late-model Godson-2 processors that have nearly the same GS464 core as the Godson-3. At Hot Chips, ICT showed slides comparing the performance of an 800MHz Godson-2F with an 850MHz Intel Pentium III. Overall, the Godson-2F was only 18% as fast as the Pentium III when running the SPEC2000 CPU benchmarks. Integer performance was 15% as fast, and floating-point performance was 21% as fast.

According to ICT's claims at Hot Chips, the Godson-3 will run x86 software more than twice as fast as the Godson-2 does. That may be fast enough for occasionally running x86 software that isn't mission critical. However, barring a breakthrough in dynamic binary translation that has eluded other computer scientists for decades, the Godson-3 will be no substitute for a real x86 processor.

Godson-3's Place in the MIPS Universe

Overall, the GS464 processor core compares favorably with other MIPS-compatible cores. MIPS Technologies stopped designing new workstation/server chips about ten years ago, so the apex from the company that invented the MIPS architecture was the R10000 of 1995. (A few subsequent microprocessors were minor enhancements of the R10000.) Like the GS464, the R10000 had four-way superscalar execution, out-of-order execution, and speculation. The R10000 had smaller L1 caches than the GS464 (32KB vs. 64KB) but a larger TLB (128 entries vs. 64).

MIPS now focuses exclusively on synthesizable embedded-processor cores. Those cores favor smaller gate counts, lower power consumption, and easy ASIC integration, although they rank among the highest-performance embedded-processor cores. The most powerful core from MIPS is the MIPS32 74K, a 32-bit processor with two-way superscalar execution and out-of-order execution. (See *MPR 5/29/07-01*, "MIPS 74K Goes Superscalar," and *MPR 6/4/07-01*, "MIPS 74K Performance Update.")

A few MIPS architectural licensees continue to design high-throughput MIPS-compatible cores for their own chips, although they've been relatively quiet lately. In 2005, Raza Microelectronics (RMI) introduced the MIPS64-compatible XLR core and XLR-family network processors. The XLR core is uniscalar and four-way multithreaded—just the opposite of the GS464, which is four-way superscalar and

single threaded. RMI packs up to eight XLR cores per chip. (See *MPR 5/17/05-01*, "A New MIPS Powerhouse Arrives.")

In 2004, Cavium Networks—another MIPS architectural licensee—designed its own MIPS64-compatible processor core, the CnMIPS64. It's a fairly conservative design, with two-way superscalar execution, in-order execution, and single threading. Optimized for networking and communications, it dispenses with an FPU and has smaller L1 caches and TLBs than the GS464 does. However, Cavium crams up to 16 of these cores on its chips, bolstered with extensive application-specific logic. (See *MPR 7/16/07-01*, "Cavium Stalks Storage," and *MPR 10/5/04-01*, "Cavium Branches Out.")

Custom MIPS64-compatible cores also appear in networking and communication chips from Broadcom and PMC-Sierra, but they are aging. Broadcom gained the four-way superscalar SB-1 core by acquiring SiByte in 2000 and has built only a few chips around it. Broadcom's dual-core BCM1280 and quad-core BCM1480 remain available but haven't been updated since 2004. PMC-Sierra introduced the two-way superscalar E11K core in 2004, but it was a relatively minor enhancement of PMC-Sierra's older E9K core. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.")

Godson-3's Place in the CPU Universe

After every Godson announcement, *MPR* fields questions from reporters asking how the Chinese processor stacks up against microprocessors from Intel and other CPU vendors. It's a tough question.

For one thing, the MIPS architecture is no longer at the forefront of PCs, workstations, servers, and supercomputers, so there are no MIPS-compatible processors directly comparable with Godson. To a certain point, comparisons with other CPU architectures are valid, but Godson isn't intended to compete against leading CPUs in the world market (yet). Because Godson is intended mainly for Chinese domestic consumption, design priorities revolve around the somewhat different requirements of the Chinese market.

The Godson-3 is the most ambitious Godson generation yet seen. Its architects hope to adapt the basic design to everything from small embedded systems to supercomputers. Their goal seems overreaching and clouds any comparisons still further.

Strictly speaking, the Godson-3 microarchitecture is more imitative than innovative. But then, we haven't seen any breakthroughs at the microarchitectural level from anyone in years. In general, the past few years have been a period of retrenchment against the intolerable rise of power consumption. High-performance processor cores are often getting simpler, not more complex. CPU architects are improving performance by replicating simpler cores in larger-scale multicore chips.

One exception to the status quo in microarchitecture is chip multithreading. This technique isn't new, either, but it's gaining momentum across diverse product lines. Dual Hyper-Threading has reappeared in more of Intel's processors lately, including Atom, and Intel's future Larrabee processors will support four threads per core. (See *MPR 4/7/08-01*, "Intel's Tiny Atom," and *MPR 9/29/08-01*, "Intel's Larrabee Redefines GPUs.") In 2006, MIPS introduced the first synthesizable processor with hardware multithreading, and this year followed with another multithreaded core. (See *MPR 2/27/06-01*, "MIPS Threads the Needle," and *MPR 4/28/08-01*, "Multicore Multithreading With MIPS.") Sun Microsystems has been particularly aggressive in this regard. Its eight-core UltraSPARC T2 server processor supports eight threads per core. (See *MPR 12/10/07-01*, "Server Processors: Chapter 2007 [Part 2].")

In view of these trends, it may seem surprising that the GS464 core in the Godson-3 is single threaded. Indeed, when

Price & Availability

The first version of the Godson-3 will have four MIPS-compatible GS464 processor cores and is expected to tape out later this year. In 2009, the second version of the Godson-3 will integrate four GS464 cores with four GStera coprocessors. Godson processors are usually marketed commercially under the Loongson or Dragon names. No prices or availability dates have been announced. For more information, visit the following websites:

x86 FPU optimizations in the Godson architecture:

- *www.ict.ac.cn/grope/down/07-09/1189478389.pdf*
- *www.ict.ac.cn/grope/down/07-09/1189478291.pdf*

Additional Godson-related topics:

- *www.ict.ac.cn/grope/down/08-01/1199358764.pdf*
- *http://jcst.ict.ac.cn/ptafile%5C3998.pdf*
- *http://jcst.ict.ac.cn/content/papere.asp?lg=en&i=7101*
- *http://jcst.ict.ac.cn/content/papere.asp?lg=en&i=8214*
- *http://jcst.ict.ac.cn/content/papere.asp?lg=en&i=6501*

Institute for Computing Technology, Chinese Academy of Sciences:

- *www.ict.ac.cn*
- *www.ict.ac.cn/english/international/channel/2449.shtml*

Chinese Journal of Computers:

- *http://cjc.ict.ac.cn/eng/index.htm*

QEMU dynamic binary translator:

- *http://bellard.org/qemu/*

EMTEC Gdium netbook PC:

- *www.gdium.com*

HiVision Mininote PC:

- *http://gizmodo.com/5047705/hivision-shows-off-sub+100-linux-mini-laptop*

Lemote Fuloong PC:

- *www.lemote.com/english/fuloong.html*

The video of ICT's presentation at the Hot Chips Symposium is available on DVD:

- *www.hotchips.org/hc20/main_page.htm*

MPR met with Godson architect Weiwu Hu at his Beijing lab in 2006, he hinted that the Godson-3 would be multithreaded. Of course, the Godson-3 was a whiteboard project at that time. In the two years since then, Hu apparently decided against making major alterations to the microarchitecture. The GS464 is little changed from the Godson-2 core, except for full MIPS64 compatibility and the x86-translation instructions. Instead, ICT is turning its attention to multicore—enough challenge for a new-generation design.

Considering ICT's ambitions for the Godson-3, the emphasis on multicore is justified. ICT needs a highly scalable building block that spans the gamut from embedded systems to supercomputers. Scaling the number of cores is the only practical path toward that goal. Chip multithreading is a refinement that will likely find its way into future Godson processors. In 2007, ICT published a paper in the *Journal of Computer Science and Technology*, titled "Chip Multithreaded Consistency Model." The paper describes a hypothetical multithreaded version of the Godson-2 processor.

Outlook for the Godson-3

Although *MPR* regards the Godson-3 as an important advance in Chinese microprocessor design, we are skeptical that the new GS464 core is the best solution for every application envisioned for it. In most embedded systems, a 64-bit core with four-way superscalar pipelining and out-of-order execution is overkill. As noted above, even the latest PC and server processors are embracing simpler cores that are easier to replicate. In most massively parallel designs, the processor cores are simpler still, with 16-bit engines not uncommon.

Today, Intel has four distinct x86 microarchitectures in production or approaching production. Yet Intel's spectrum of target applications is narrower than the Godson-3's. Intel is targeting mobile Internet devices, netbooks, PCs, servers, and supercomputers. The GS464 microarchitecture is supposed to address that same spectrum, plus smaller embedded systems. We suspect that ICT will eventually develop simpler cores to compete with ARM and MIPS at the low end.

The new XBAR extensions for accelerating x86-to-MIPS translation on the Godson-3 are intriguing. Judging from the information available, the extensions probably don't infringe on Intel's or Transmeta's intellectual property, but patent lawyers for those companies may have a different view. It could be a moot point if Godson-3 processors stayed in China, but some will probably be exported to world markets. Removing the extensions from an export version of the core shouldn't be difficult.

One measure of Godson's importance to China is the resources assigned to the project. According to Zhiwei Xu, the ICT professor who presented the Godson-3 at Hot Chips, the hardware-design team has about 200 people. The compiler team has another 50 people, and an equal number are working on other software-development tools and system software. The 300-member Godson team easily outnumbers the total number of employees at MIPS Technologies (not counting the company's Chipidea subsidiary in Portugal). In addition, about 40 Chinese companies are developing software for Godson, according to Xu.

Like everything happening in China, Godson bears watching. As the Chinese develop better microprocessor technology, they will have less need to import foreign microprocessors. It seems inevitable that someday the Chinese will export microprocessors in sufficient quantity and of sufficient quality to challenge the world's established chipmakers. ◇