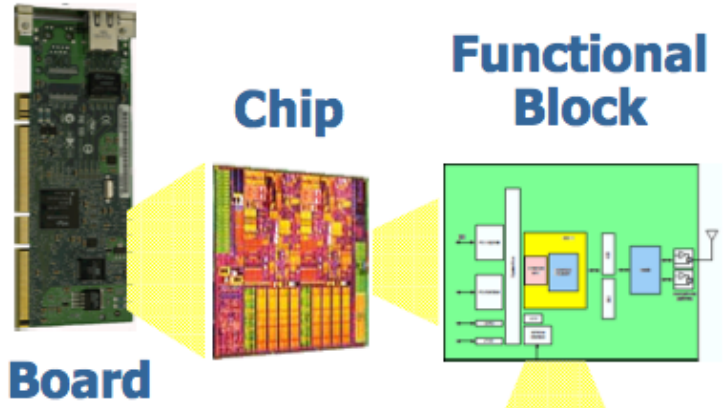
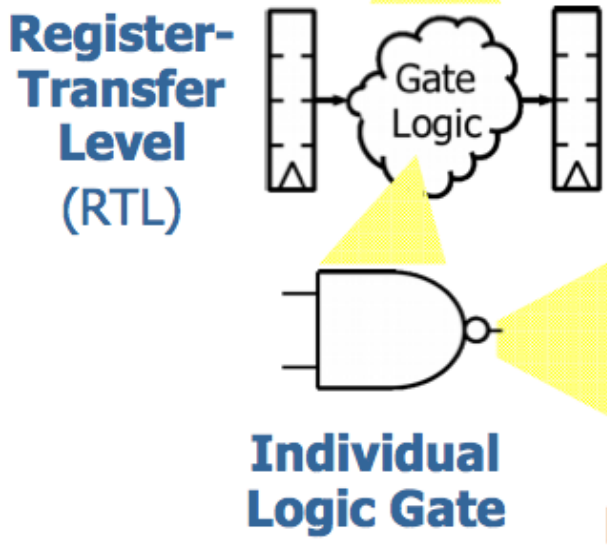
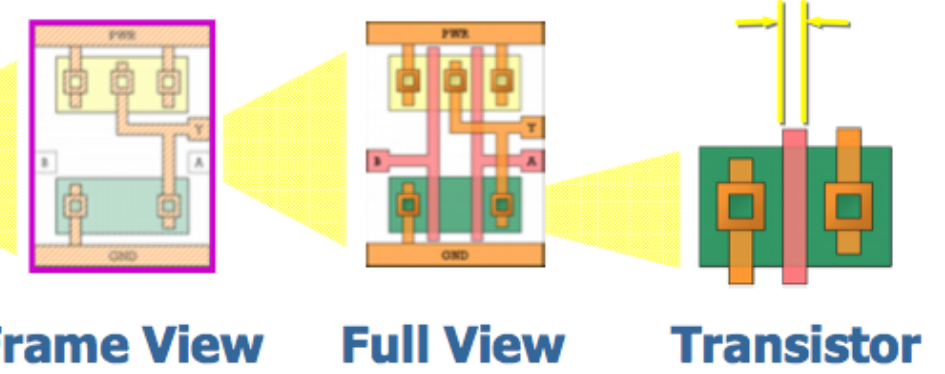
Selected slides from Nanometer ASIC couse slides developed by Charles Dancak

Managing Complexity



Key Principle:
SOC complexity managed by working at the highest levels of abstraction, and hiding lower-level details.

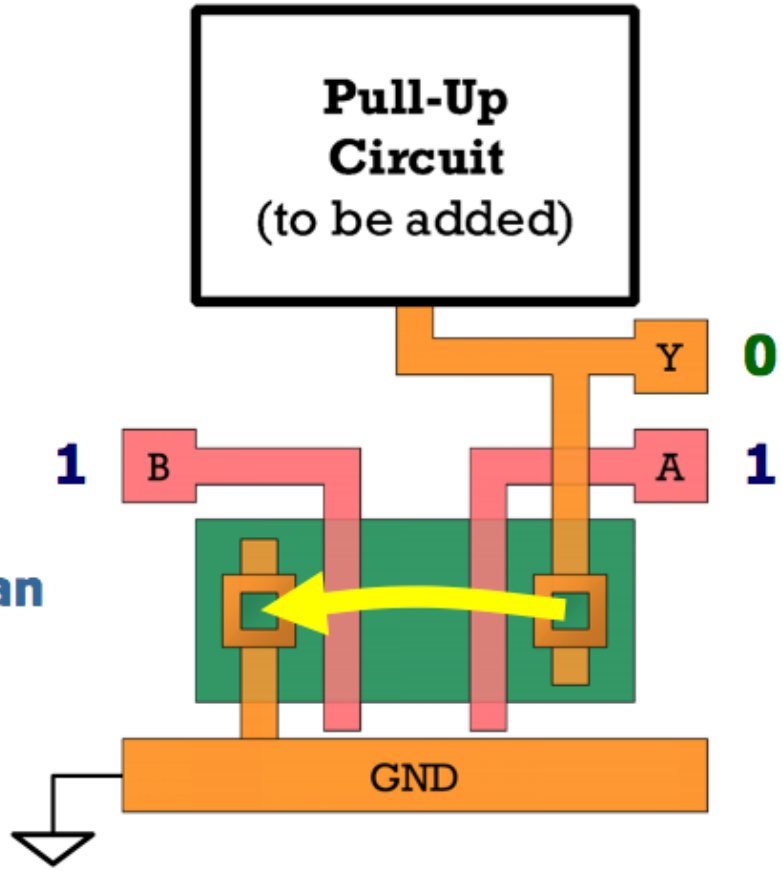




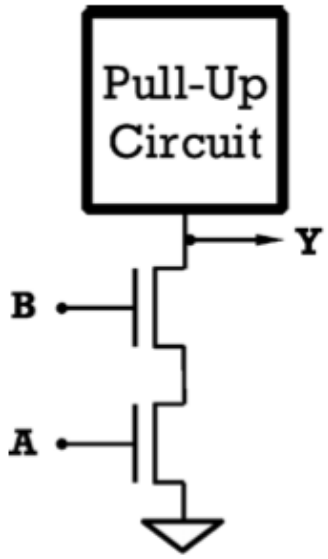
At the physical layout level, dimensions are truly nanoscale.

NAND Switching Action

NAND Table		
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Floorplan View

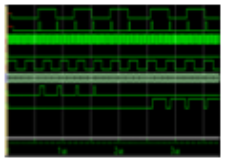


$Y = \sim(A \& B)$

- Two transistors in series implement NOT-AND action.
- When A and B are 1, the output Y is pulled down to 0.
- In all other cases, Y gets pulled up to 1 (not shown).

Six Critical Phases

1. Specify:
State IC design intent on paper.



3. Verify:
Confirm that RTL code reflects original intent.

1. Specify

2. Design

3. Verify

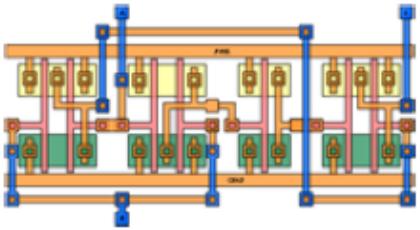
4. Implement

5. Fabricate

6. Qualify

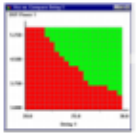
2. Design:
Realize design intent by describing digital logic at RTL level.

4. Implement:
Synthesize RTL code into 32-nm standard cells. Place and route.



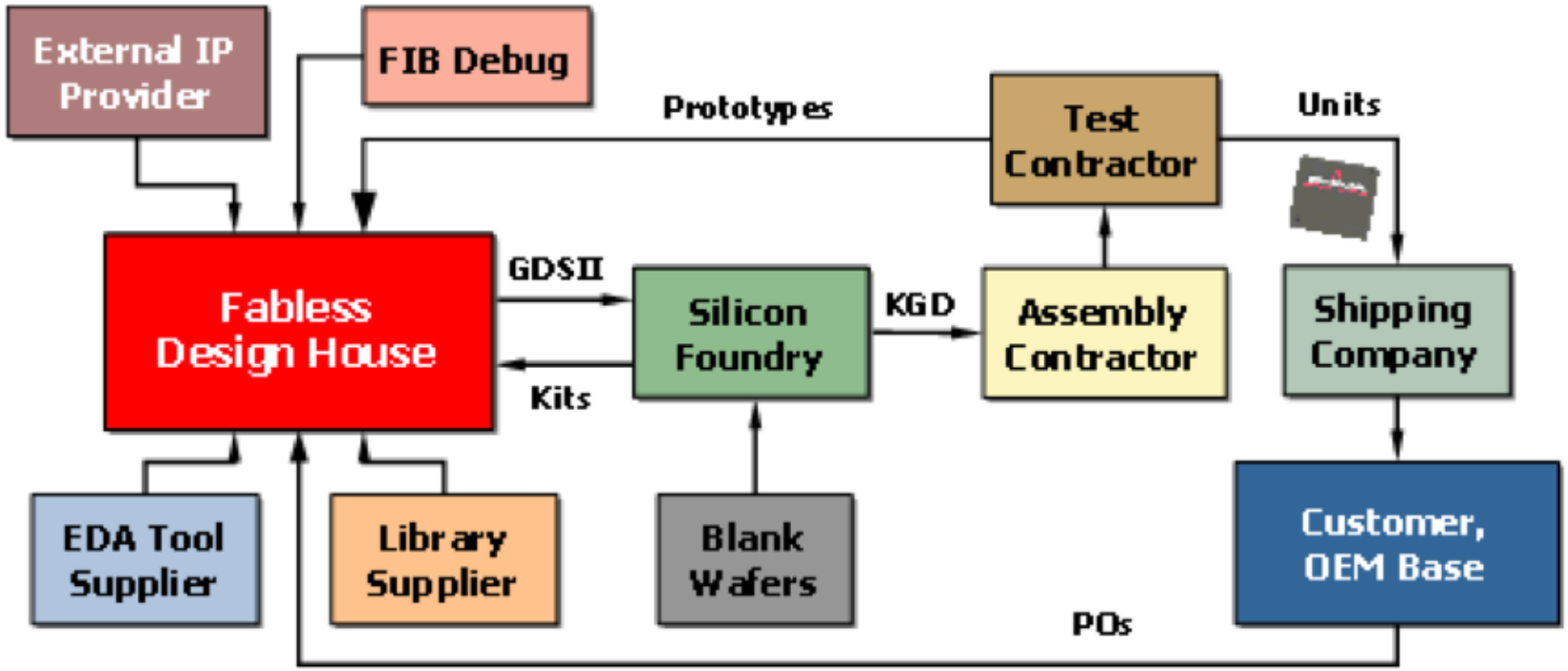
5. Fabricate:
Create mask set. Imprint each layer on silicon surface.

6. Qualify:
Validate IC for customer use.



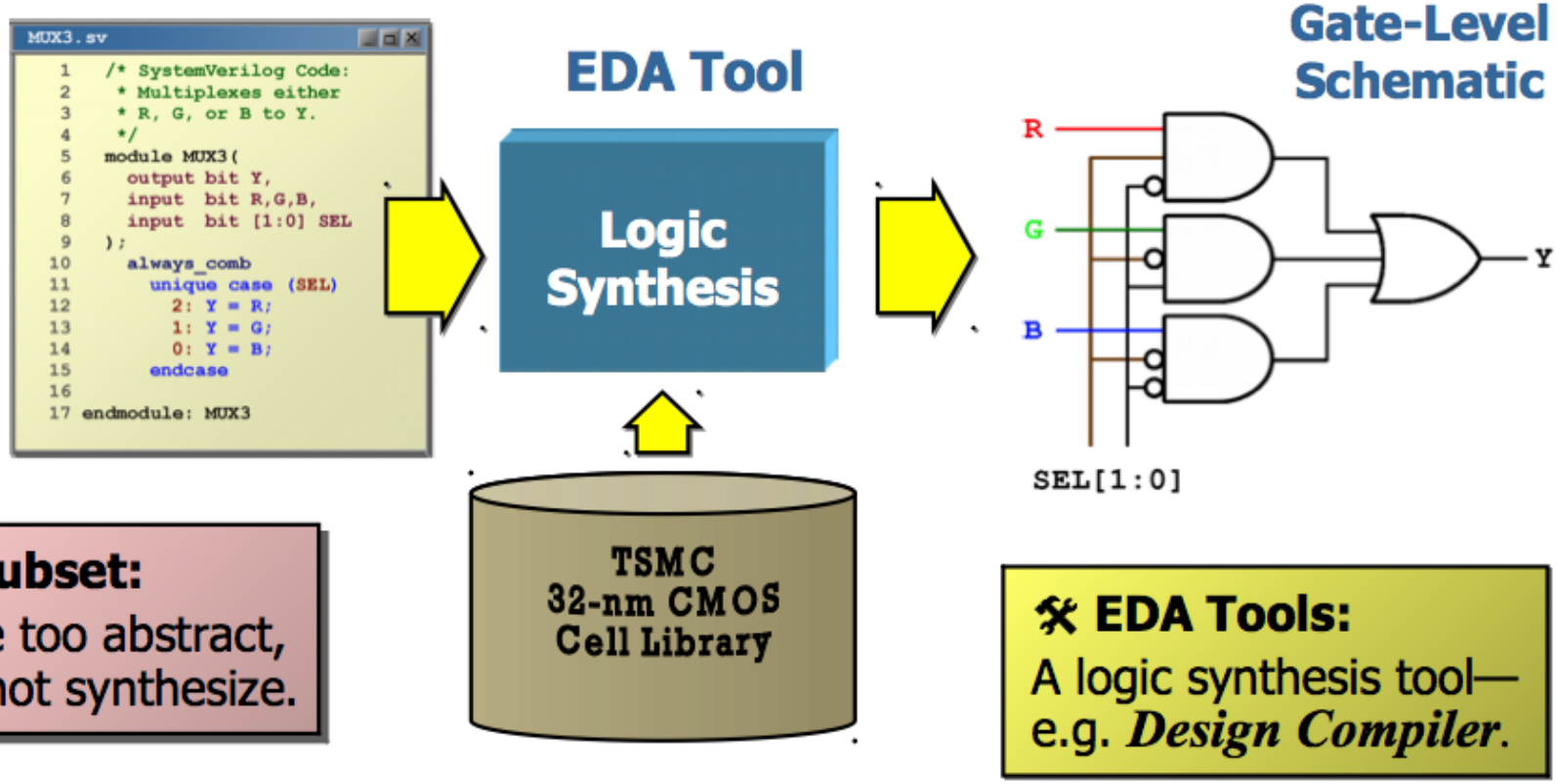
- **Developing a new ASIC involves hundreds of steps.**
- **We'll subdivide them into these six distinct phases.**

The ASIC Ecosystem



- A **fabless** design house focuses on design innovation.
- In-house experts may still work closely with **foundry.**
- Project planning secures **commitments** of partners.

HDL-Based Synthesis



RTL Subset:
If code too abstract, it will not synthesize.

🛠 EDA Tools:
A logic synthesis tool—e.g. ***Design Compiler***.

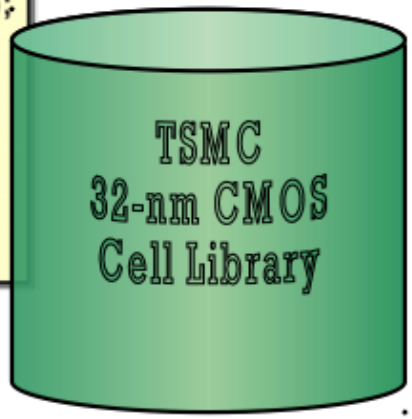
- **The synthesis tool is able to read in an HDL code file.**
- **It compiles the HDL constructs into equivalent logic.**
- **Optimizes for speed—then trims down overall area.**

Standard-Cell Library

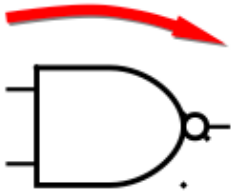

```
cell (ND2_1) {
   area: 3.0;
   pin (Y) {
      direction: output;
      function: ~(A & B);
      timing ( ) {
         related_pin : A;
         delay {0.012,...}
      }
   }...
}
```

Liberty Format

tsmc_32nm.lib

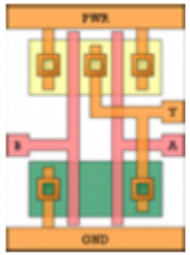


Pin-to-Pin Delay (τ_{gate})



Power Usage

Cell Area



$$\tau_{gate} \approx \tau_{intrinsic} + \tau_{load} + \tau_{slew}$$

Key Principle:
Cells characterized by SPICE simulation and foundry runs.

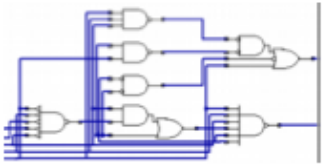
- **Synthesis tool accesses a foundry-specific cell library.**
- **Most cells come in drive strengths from ×1 up to ×16.**
- **Cell characteristics listed in concise *Liberty* format.**

IP Core Formats

Soft IP
(RTL Code)

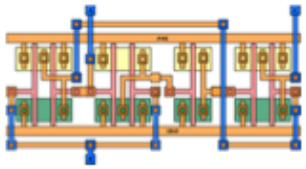
Aspects:
- User-modifiable.
- Synthesized with other RTL code.

Firm IP
(Netlist)



Aspects:
- Fine-tuneable.
- Can be resynthesized to a user's constraints.

Hard IP
(Layout)



Aspects:
- Optimized to technology.
- Not modifiable by user.
- Physical design by vendor.

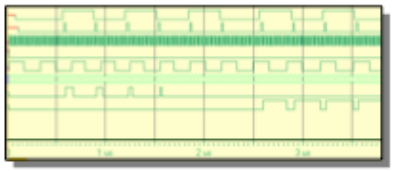
IP Economics:
Hard IP can be 10× cheaper because it's less user-modifiable. Soft IP is modifiable —but vendor defends the product branding.

- **Usually ARM and similar IP provided in soft format.**
- **Analog or high-speed digital interface is always hard.**

Verification Trends

RTL Code

Overall Verification Strategy



Traditional Simulation
(Subtopic 3.2)

Formal Checking
(Subtopic 3.4)

Directed Testcases

CRV with Functional Coverage

(Subtopic 3.3)

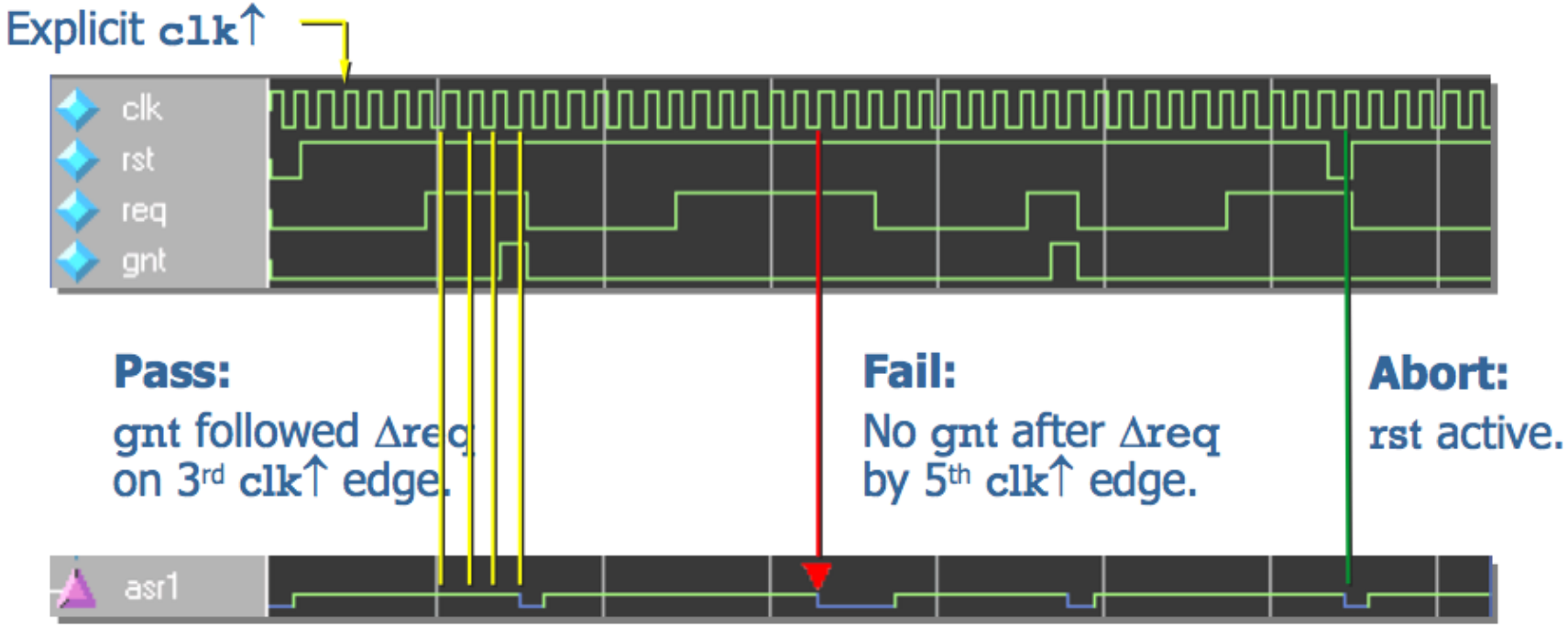
Assertions
(SystemVerilog)

Hardware Emulation
(Subtopic 3.5)

Embedded Assertions

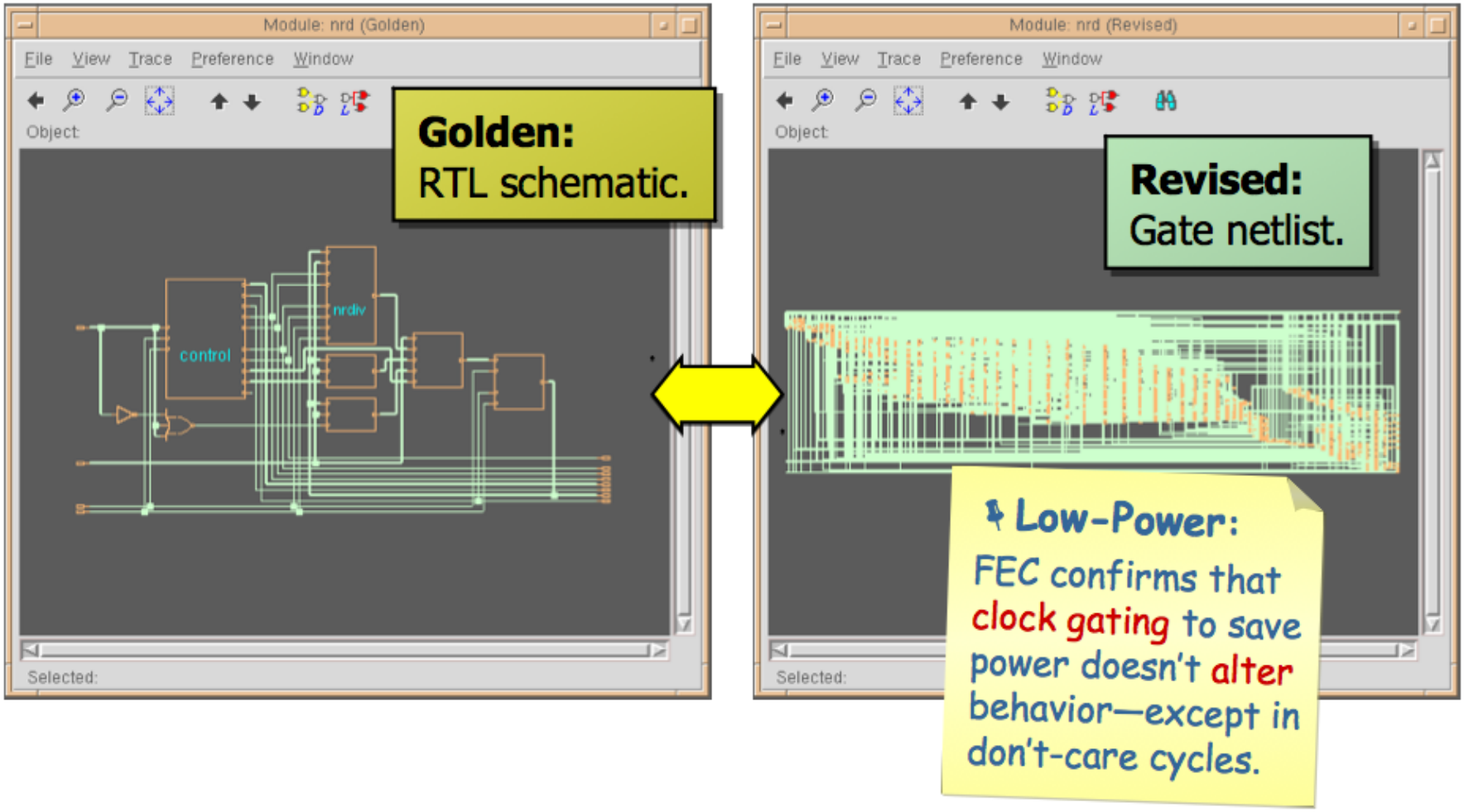

```
//Declare property:
  property req5gnt;
    @(posedge clk) disable iff (!rst)
    $rose(req) |-> ##[1:5] gnt;
```

```
//Assert concurrently:
  assert property (req5gnt);
```



- **Assertion checked every clock edge; failures logged.**
- **Property asserted can be entire sequence of events.**

A Successful Check



- **These RTL and gate-level schematics seem different.**
- **But were proven functionally equivalent by FEC tool.**

Emulation Concepts

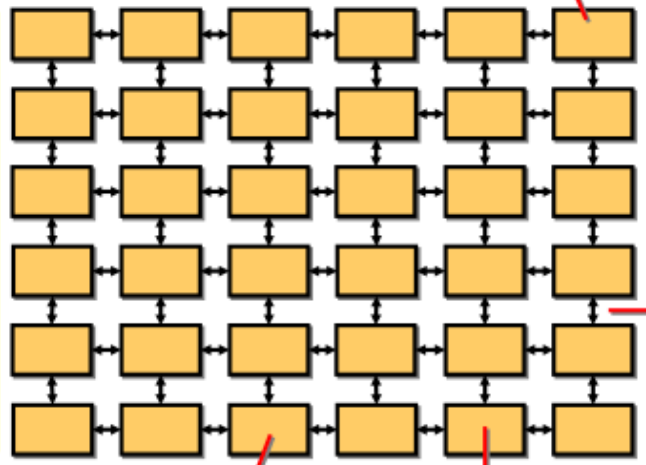
EDA Tools:
HW Emulator

```
//Short counter:
always_ff @(posedge CLK)
  if (SEL!=2) ++SEL;
  else SEL = '0;
```

RTL Construct

Not At Speed:
Runs at ~10 MHz. Slower than rated speed, but faster than any simulator.

Emulator Platform



Event Signaling

Assertion

Gate-Level

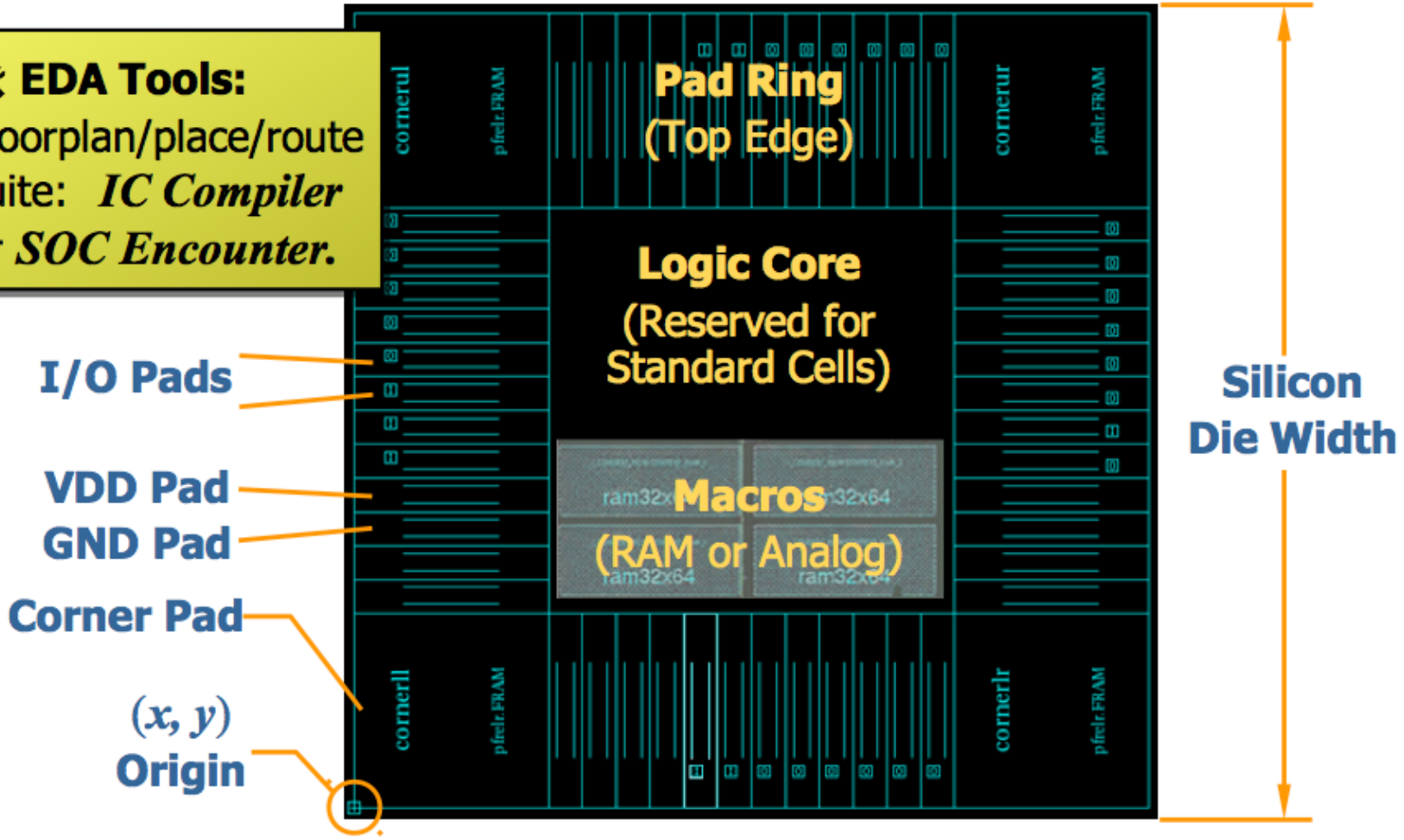
```
//Buffer instance:
  TRIBUF T0(OUT,IN,~OE);
```

```
//Detect invalid item:
  assert property (SEL!=3);
```

- **HDL code compiled, mapped onto FPGA-like clusters.**
- **Huge array is a lower-speed hardware model of SOC.**

Initial Floorplan

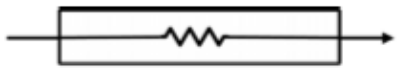
EDA Tools:
Floorplan/place/route suite: *IC Compiler* or *SOC Encounter.*



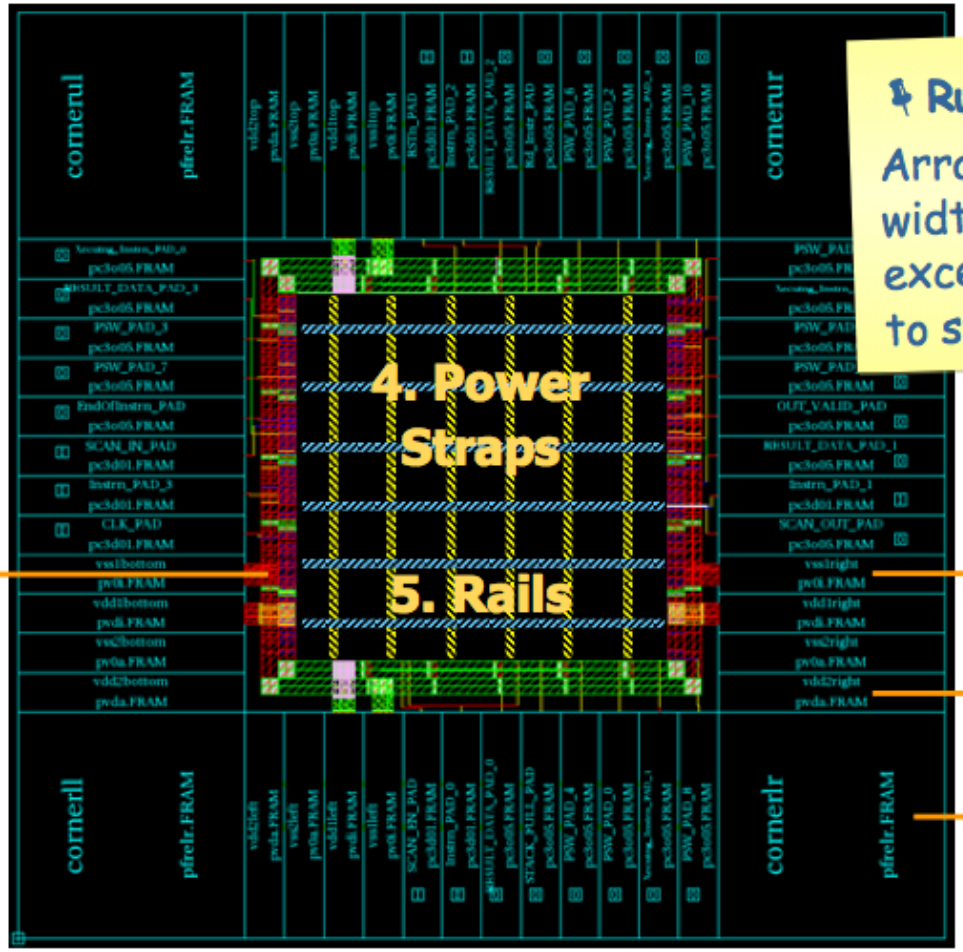
- **A floorplan arranges all blocks within an outline of silicon die.**
- **Routing regions required in between the pad ring and core.**

Power-Supply Grid

Ohmic Drop



$$\Delta V = IR_{net}$$



3. Supply Rings
(Layers M3, M4)

1. VSS Pad

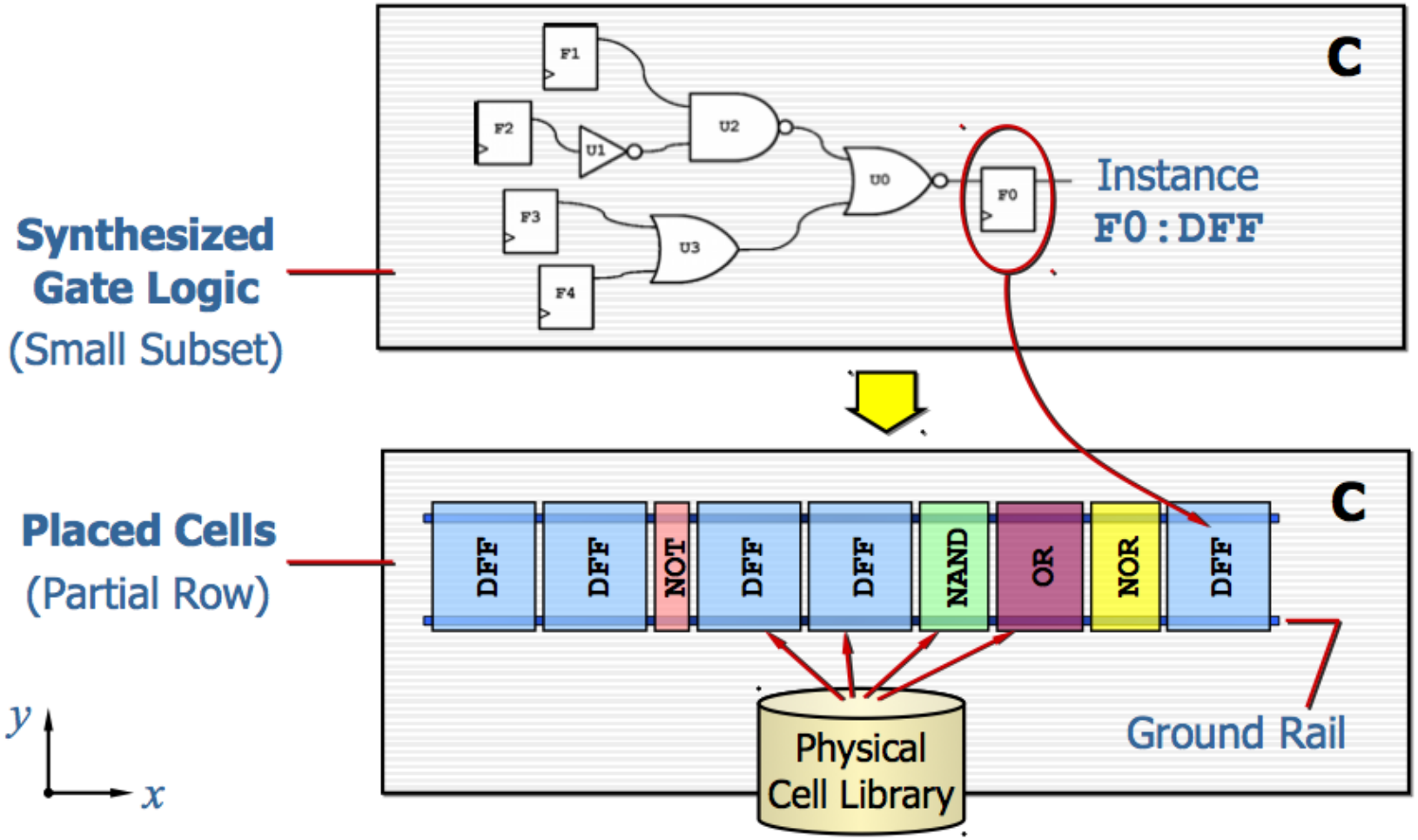
1. VDD Pad

2. Corner Pads

Rule of Thumb:
Arrange grid lines, widths to preclude excessive *IR* drop to standard cells.

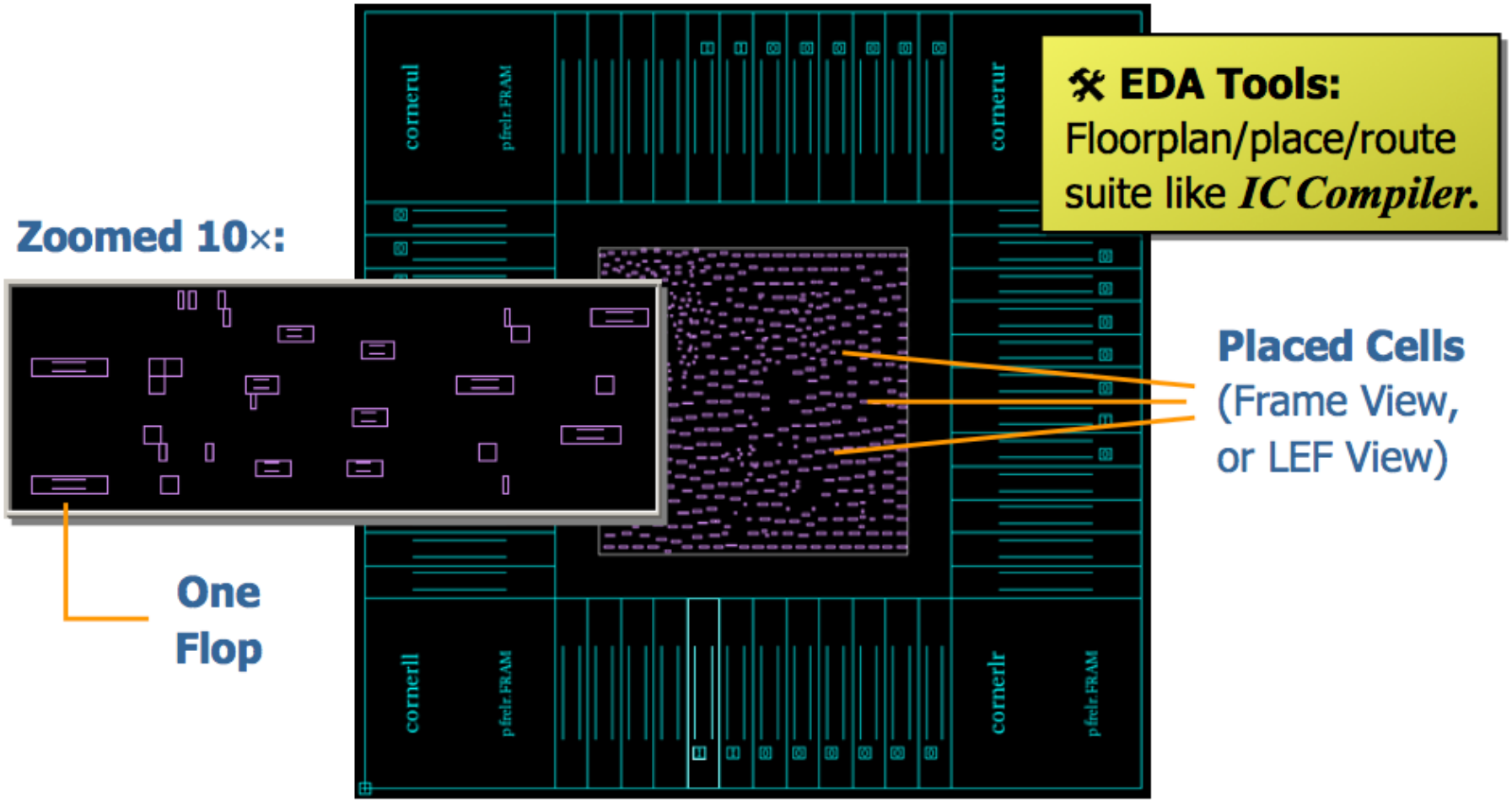
- **Floorplanning includes adding power-supply rings, straps.**
- **Supply straps in turn feed power to local standard-cell rails.**

Topological to Physical



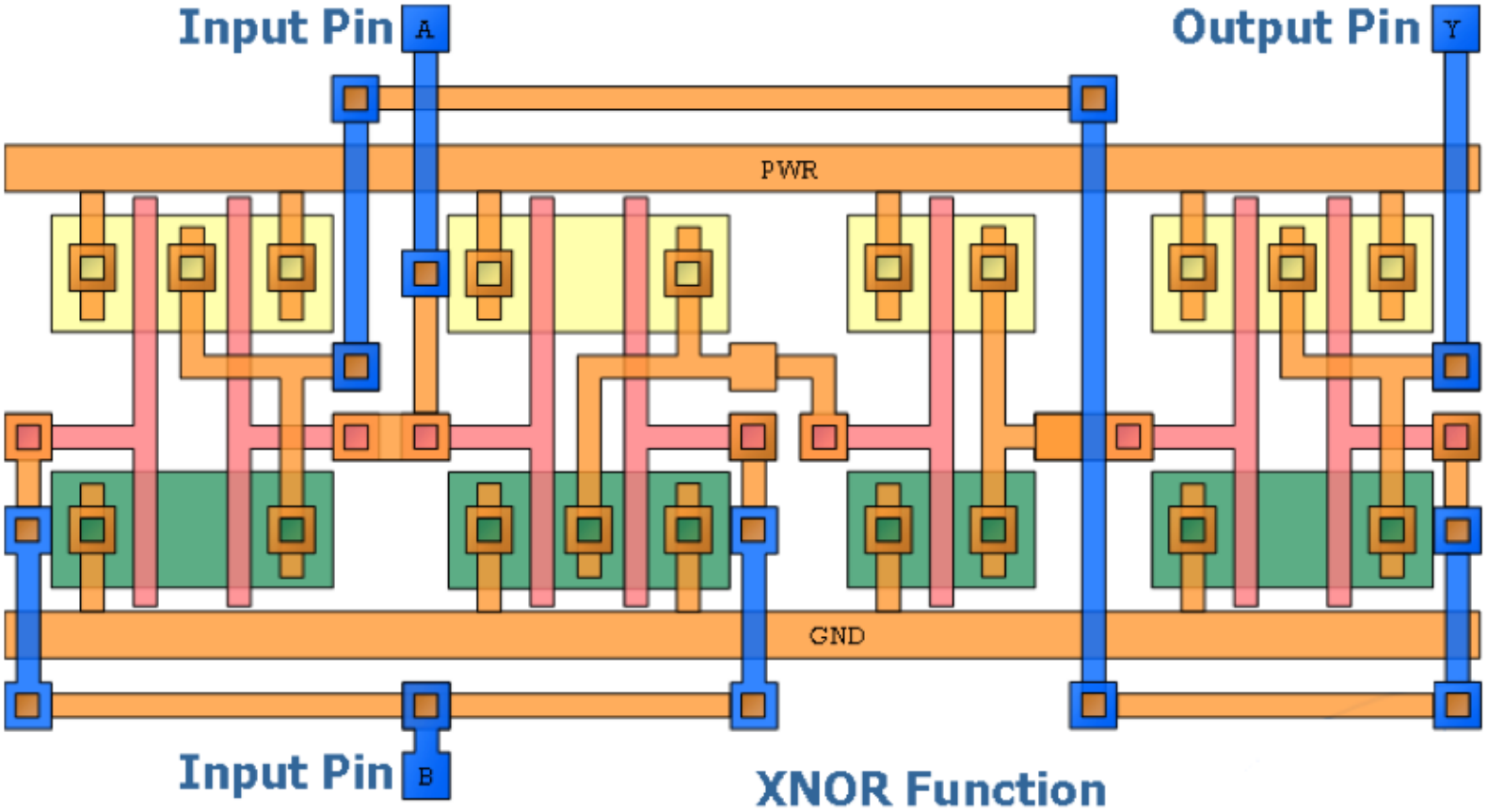
- **During placement, standard cells are positioned in rows.**
- **Voltage is distributed via common power, ground rails.**

Final Cell Placement



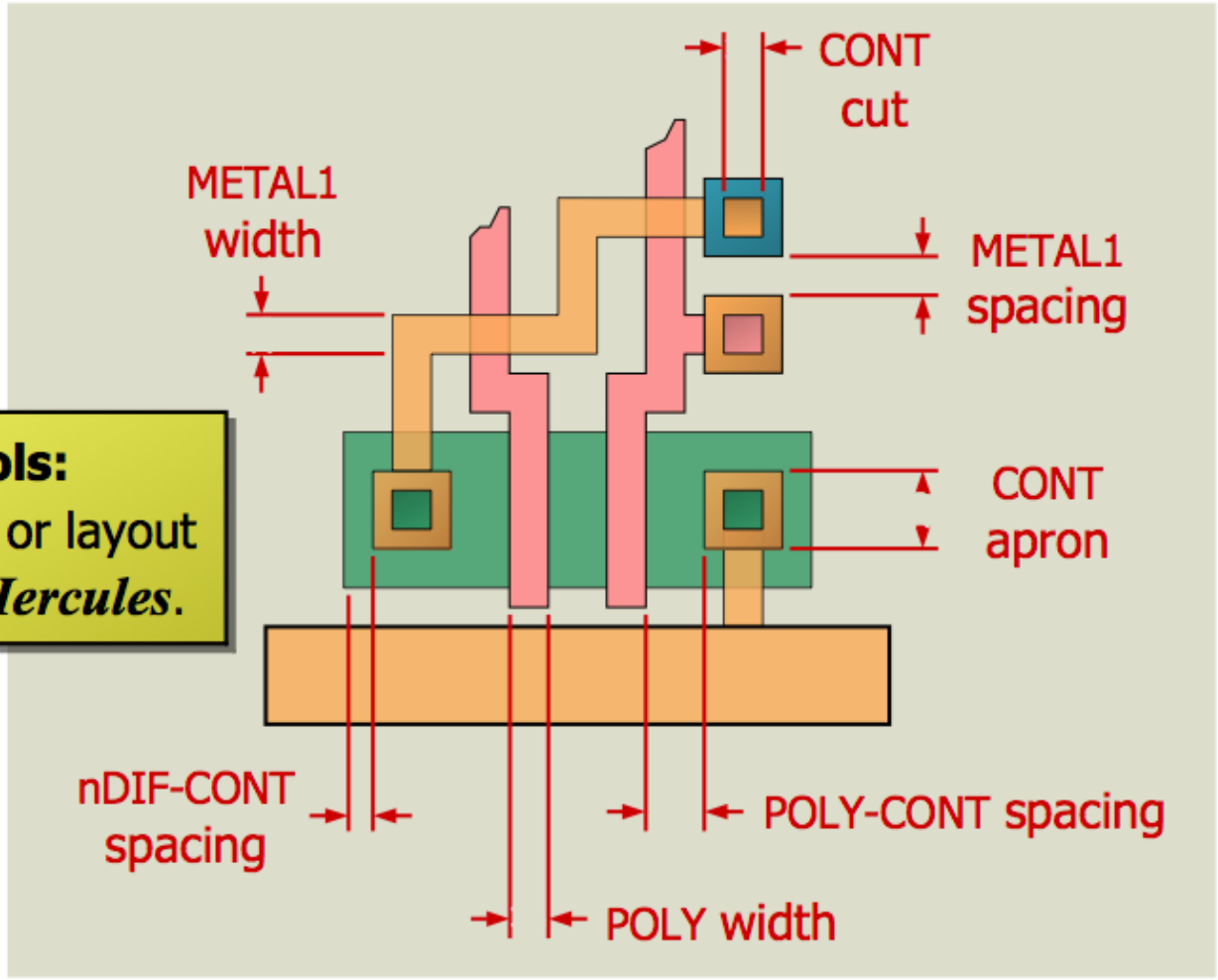
- **Every standard cell in netlist is placed at an (x, y) location.**
- **Cells arranged in horizontal rows—but not yet connected.**

Standard-Cell Routing



- Identical in height, standard cells abut to form rows.
- Router makes pin-to-pin connections on metal layers.
- Logic function shown compares two bits for equality.

Design-Rule Checking

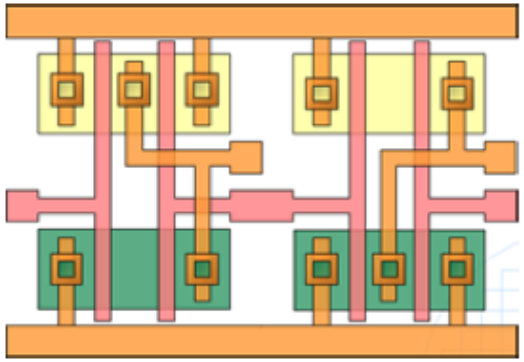


🛠 EDA Tools:
Either ***ICC***, or layout editor like ***Hercules***.

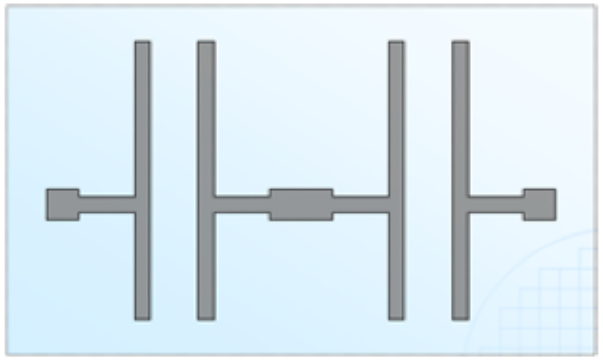
- **DRC rules determine the width and height of standard cells.**
- **Manufacturability requires strict adherence to all DRC rules.**

At the Photomask Shop

Full-Chip Geometric Database
(40–50 Layers)

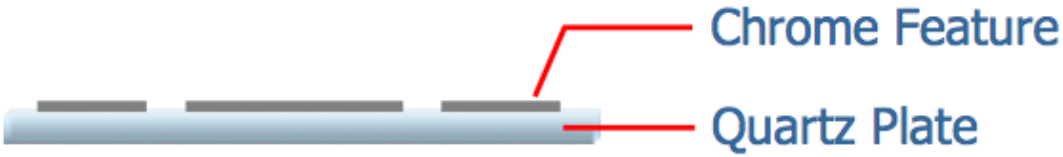


Partial Row of Cells
(NAND-NOR Gates)



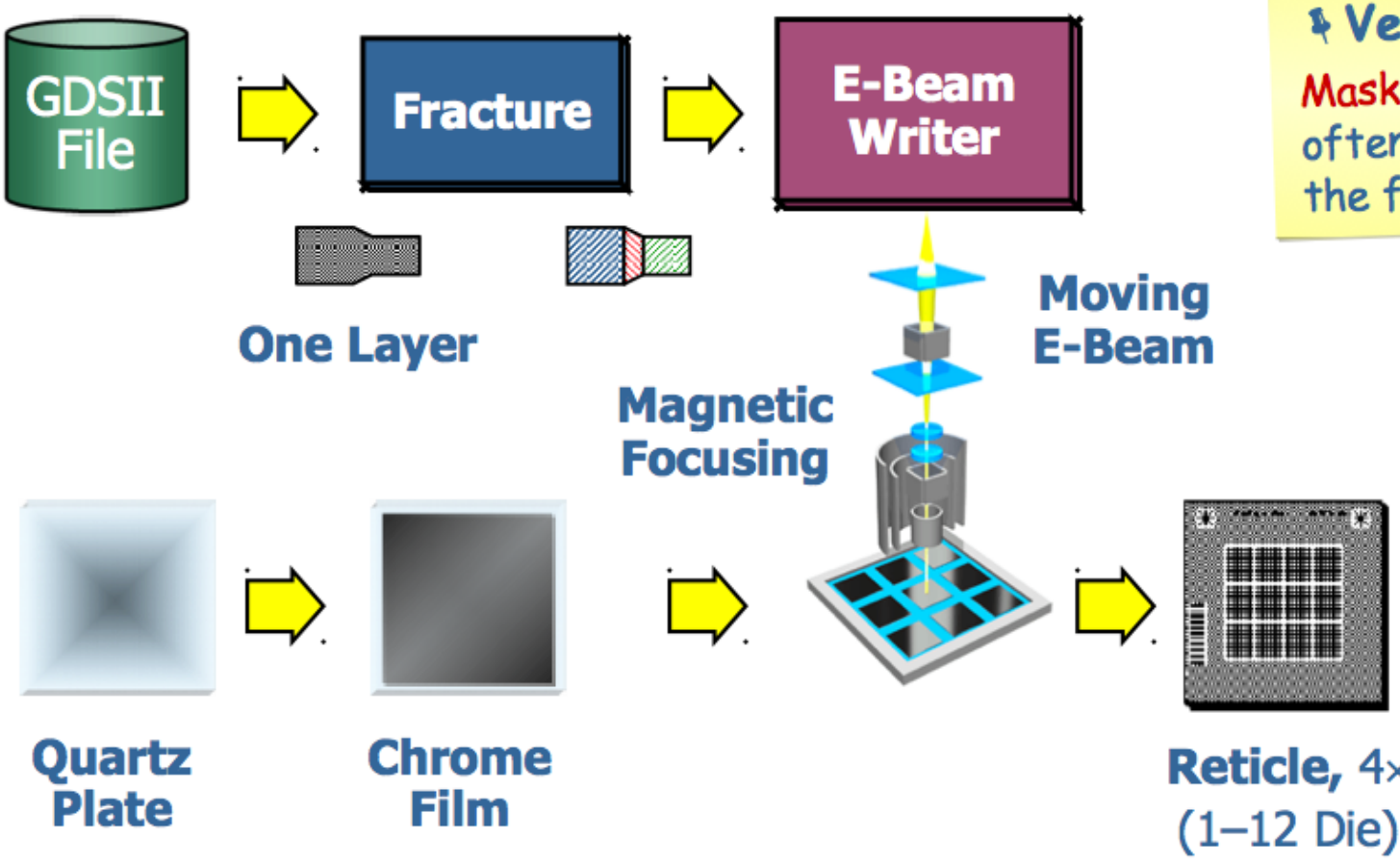
POLY Mask
Top View
(#4)

POLY Mask
Cross-Section



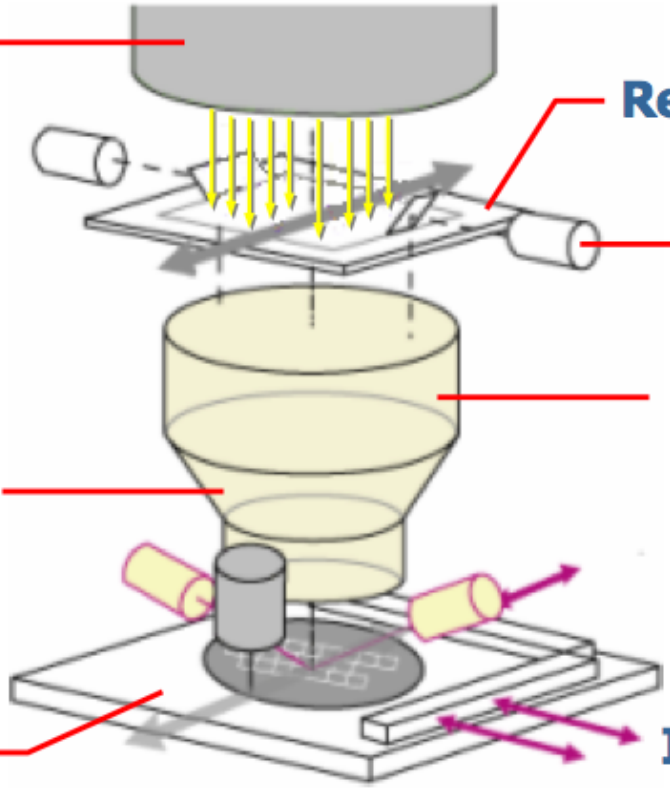
- **At tape-out, GDSII file was ftped to photomask shop.**
- **Geometry of each layer is written onto a blank mask.**

Design Data to Mask Set



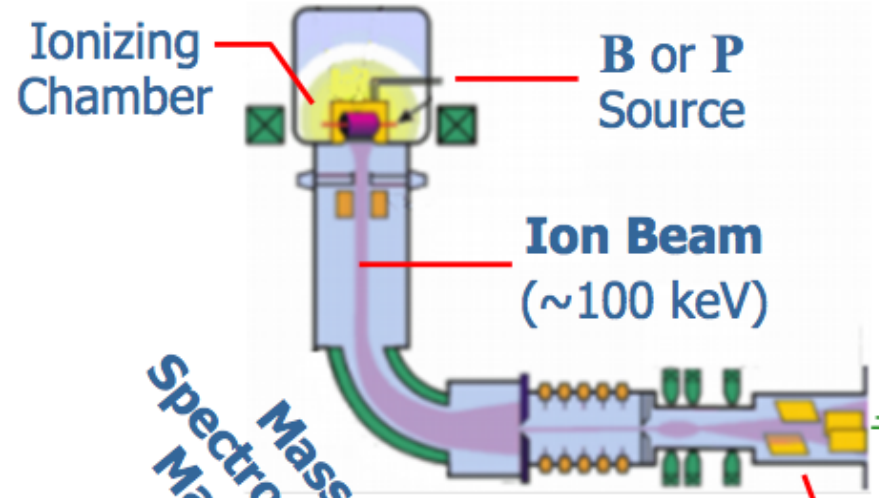
- A moving electron beam selectively removes chrome.
- Result: precise 4× pattern of geometry for one layer.

Step-and-Repeat Stage



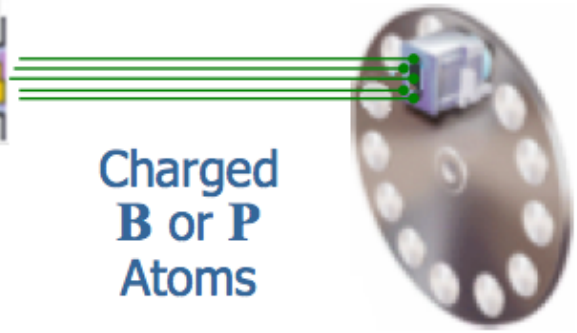
- **In earlier steppers, the reticle remained stationary.**
- **The wafer was stepped, and entire reticle exposed.**
- **A scanning stepper moves both, exposing by strips.**

Ion Implantation



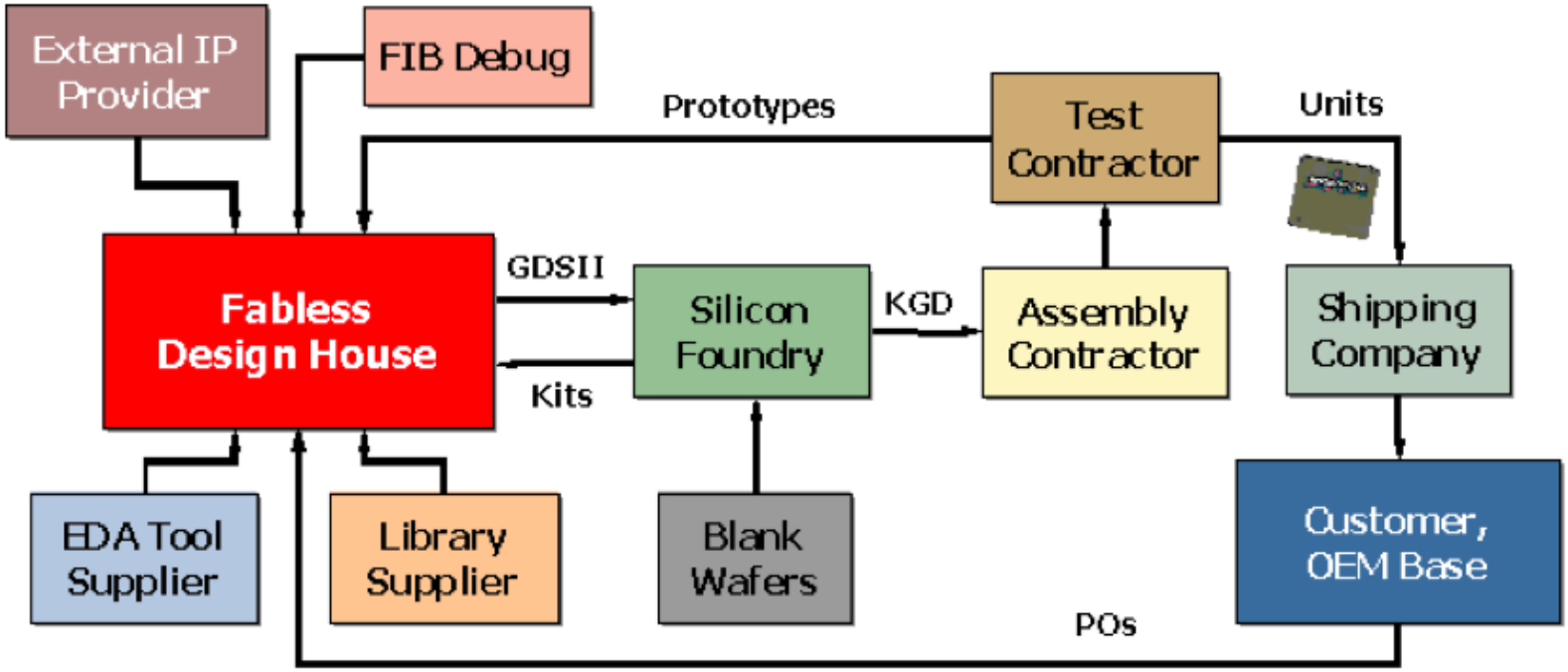
$$Q = \frac{1}{qA}\int I dt$$

Dose
(atoms/cm²)



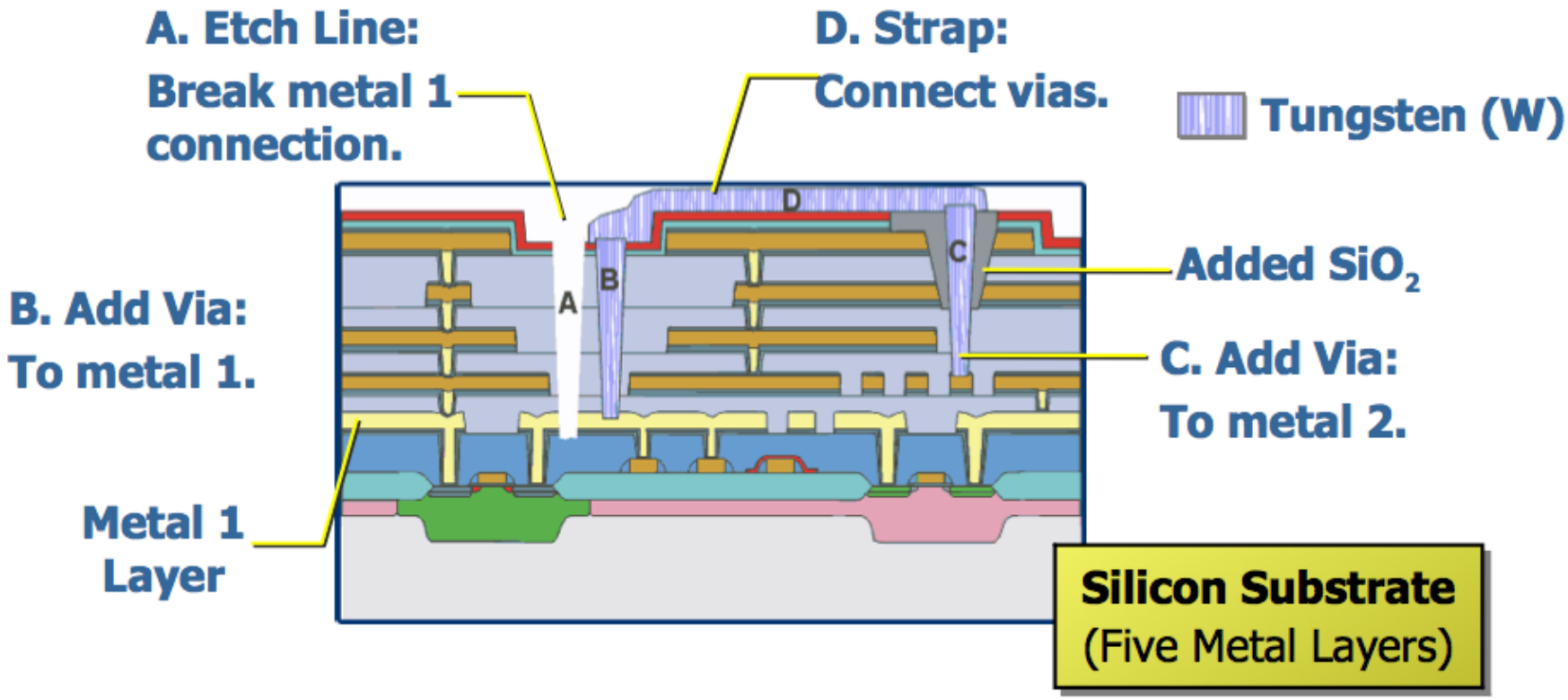
- **Implantation buries dopant atoms just below surface.**
- **Dopant profile—depth and dose—carefully controlled.**
- **Annealing resettles atoms in damaged crystal lattice.**

Economics of Wafers



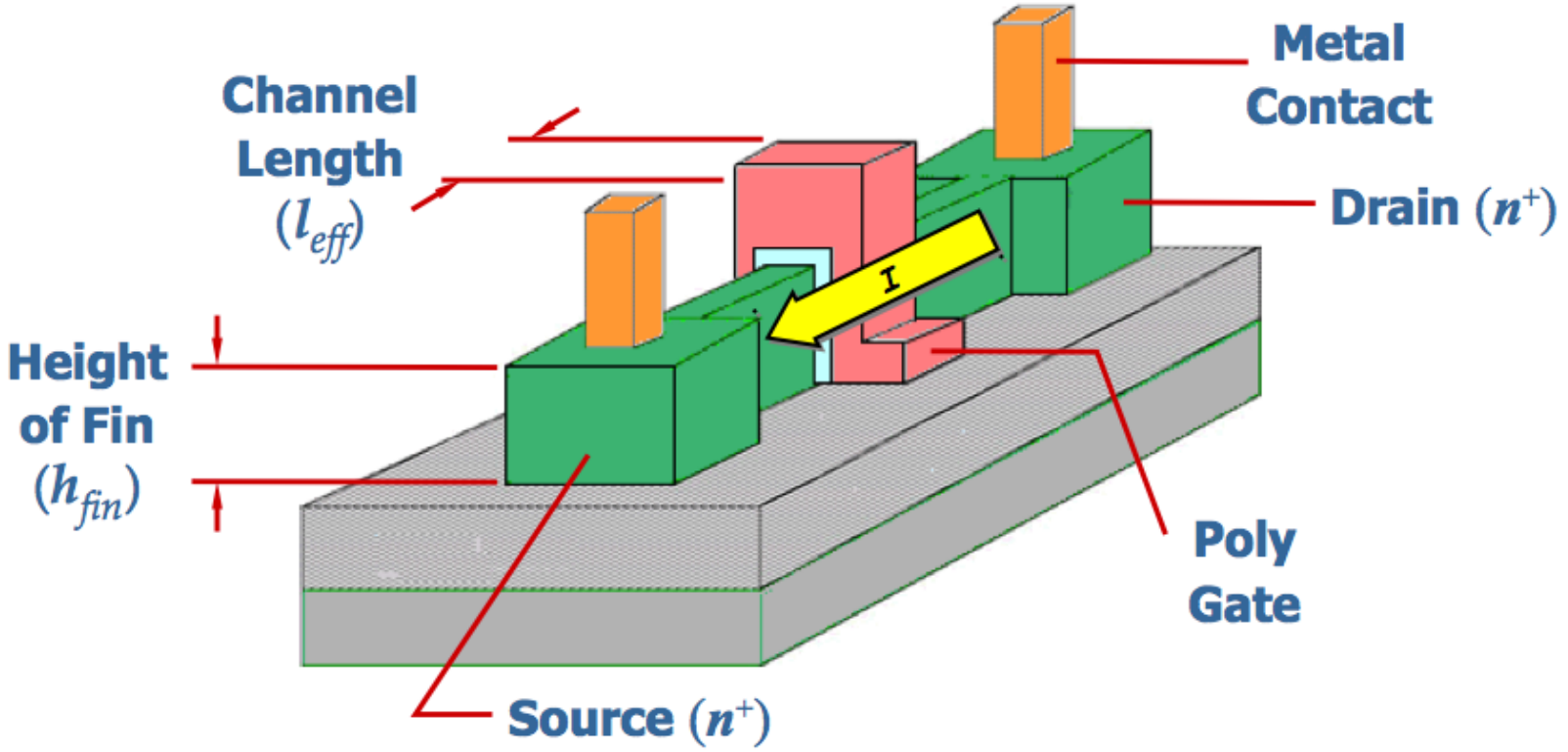
- **Foundries like TSMC buy blank wafers from a supplier.**
- **Growing defect-free silicon crystals is an art in itself.**
- **One blank 300-mm wafer costs over a hundred dollars.**

FIB Microsurgery



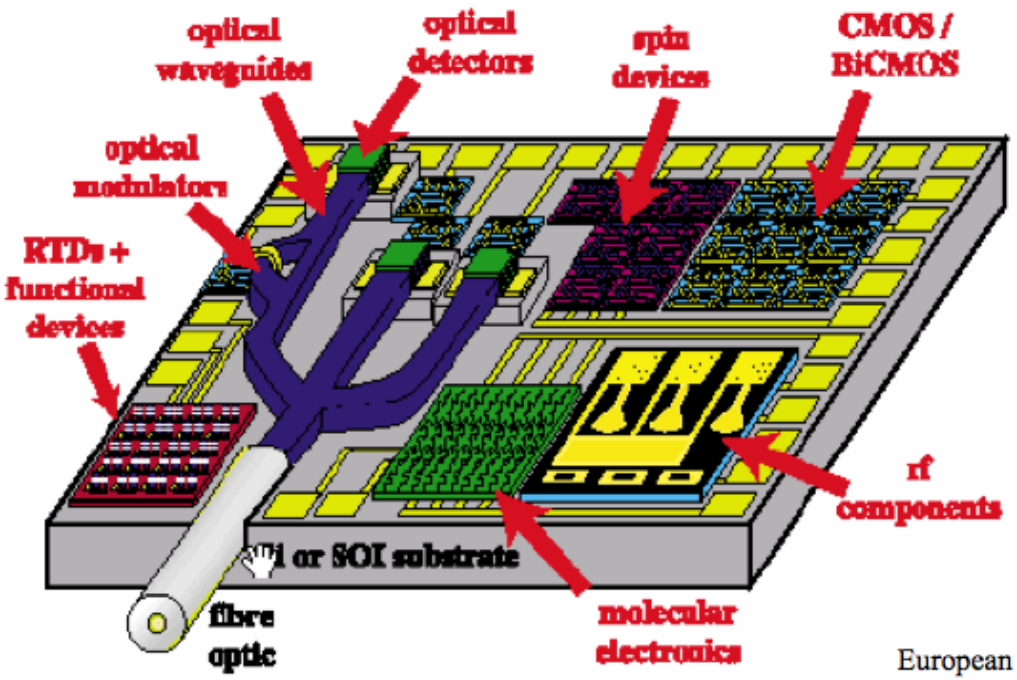
- Focused ion-beam milling is like electron microscopy.
- Heavy Ga ions edit circuitry, to prove out a mask fix.
- Often key customers want a working sample of a fix.
- Harder with flip-chip; back of the die must be etched.

Single nMOS FinFET (4/4) A-12



- Contacts are added as usual to the source, drain, and gate.
- The green-shaded ends of the fin behave like the nanowire.
- The resulting finFET approaches ideal long-channel behavior.
- Structure should scale well from 22 nm to 14 nm to 10 nm.

Beyond CMOS ICs



European Nanotechnology Roadmap

Gordon Moore, **Intel** ('65)

- **Moore's Law is thus expected to continue for two decades.**
- **New devices and chip-wide interconnections may be needed.**
- **But CMOS technology will remain as a solid, scalable baseline.**